Transactions Briefs

CMOS Schmitt Trigger Design

I. M. Filanovsky and H. Baltes

Abstract—**CMOS Schmitt trigger design with given circuit thresholds is described. The approach is based on studying the transient from one stable state to another when the trigger is in linear operation. The trigger is subdivided into two subcircuits; each of them is considered as a passive load for the other. This allows the relations governing the deviations of the circuit thresholds from their given values to be obtained. The trigger device sizes are thus determined by the threshold tolerances.**

I. Introduction

The CMOS Schmitt trigger [Fig. 1(a)] is a well-known circuit. Yet, the design of this circuit has never been investigated in any detail. The circuit operation described in [1] gives a clue to some relationships between the device sizes in the circuit. However, the description is incomplete; it does not include the circuit behavior near the transition point from one stable state to another (it is simply stated that the transition is fast). A more detailed study given below introduces the additional relationships required to complete the design and choose all the device sizes.

In bipolar technology, p-n-p transistors are much slower than their n-p-n counterparts [2], and the bipolar prototype for the whole circuit of Fig. 1(a) is not known. A bipolar Schmitt trigger includes an n-p-n differential pair loaded with a resistor. As a result, the circuit analysis is simplified, and one can find approximate [3]–[5] and exact [6]–[8] calculation of the threshold voltages of this reduced circuit.

Recently [9], the analysis of an NMOS Schmitt trigger with a linear resistive load was published. The circuit of Fig. 1(a) includes two similar subcircuits (M_1, M_2, M_3 and M_4, M_5, M_6). Each of them is a highly nonlinear load for the other. However, as shown subsequently, at each transition point one subcircuit can be considered as a *linear* resistive load for the other. Then the approach of [9] becomes valid for the circuit of Fig. 1(a) as well. The results of this analysis are given here. First, they are formulated as two equations relating the device sizes to given threshold voltages. Two additional equations describe the relation between the device parameters and the threshold voltage tolerances. Finally, two inequalities relating some specific currents of the subcircuits and providing some details of the trigger I/O characteristic shape are given.

II. Current-Voltage Subcircuit Characteristics

In the circuit of Fig. 1(a), the bottom circuit M_1, M_2, M_3 (which is called here the N-subcircuit), is loaded by the top circuit, M_4, M_5, M_6 (P-subcircuit). As a result of the circuit symmetry, the inverse statement is also valid. To obtain the voltage-current characteristics of these nonlinear loads, one can take, for example, the N-subcircuit, apply a voltage source V_o, and calculate the source current I_o, assuming a constant voltage V_G at the gates of M_1 and M_2 [Fig. 2(a)].

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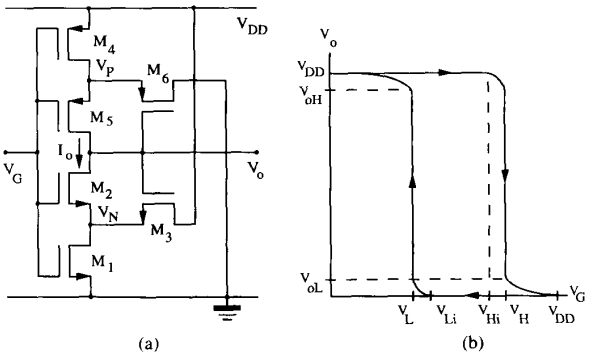

Fig. 1. CMOS Schmitt trigger and its transfer characteristic.

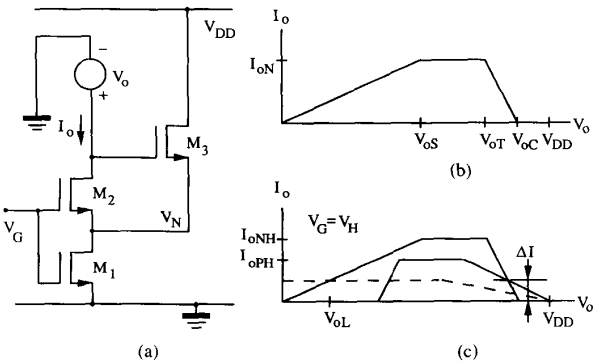

Fig. 2. N-subcircuit driven by a voltage source: (a) circuit; (b) current-voltage characteristic; (c) superposition of N- and P-subcircuit characteristics.

When the voltage V_o is very small, transistor M_3 will be *off*, and M_1 and M_2 are in the triode mode of operation. The current I_o is equal to

$$I_o = 2k_1(V_G - V_{TN})V_N \tag{1}$$

if one considers transistor M_1, or

$$I_o = 2k_2(V_G - V_N - V_{TN})(V_o - V_N) \tag{2}$$

if one considers M_2. Here $k_i = 0.5(\mu_n C_{ox})(W/L)_i$, as usual [10], and V_{TN} is the threshold voltage of n-channel transistors. For p-channel transistors, one has to use μ_p and V_{TP}. It is assumed in (1) and (2) that $V_G > V_{TN}$. For the triode mode of operation, $V_N \ll V_{TN}$ and the last equation can be simplified to

$$I_o = 2k_2(V_G - V_{TN})(V_o - V_N). \tag{3}$$

From (1) and (3), one obtains that

$$V_N = V_O \frac{k_2}{k_1 + k_2} \tag{4}$$

and

$$I_o = \frac{2k_1k_2(V_G - V_{TN})}{k_1 + k_2} V_o. \tag{5}$$

From (5) one can find that

$$R_{LN} = \left[\frac{\partial I_o}{\partial V_o}\right]^{-1} = \frac{k_1^{-1} + k_2^{-1}}{2(V_G - V_{TN})}. \quad (6)$$

It is seen from (4) and (6) that, in this part of the subcircuit operation, transistors M_1 and M_2 may be considered as a series connection of two resistors.

When V_o increases, M_2 enters into saturation (pinch-off). Then I_o is determined, depending on the considered transistor, or by

$$I_o = 2k_1[V_G - V_{TN} - (V_N/2)]V_N \quad (7)$$

or λ

$$I_o = k_2(V_G - V_N - V_{TN})^2. \quad (8)$$

From (7) and (8) one can find that

$$V_N = (V_G - V_{TN})\left(1 - \sqrt{\frac{k_1}{k_1 + k_2}}\right) \quad (9)$$

and does not depend on V_o. This means [Fig. 2(b)] that when the voltage V_o achieves the value of

$$V_{oS} = V_G - V_{TN} \quad (10)$$

the current I_o becomes constant and equal to

$$I_{oN} = \frac{k_1 k_2}{k_1 + k_2}(V_G - V_{TN})^2. \quad (11)$$

Yet, an additional increase of V_o will gradually introduce some changes. When V_o achieves the value of

$$V_{oT} = V_G - (V_G - V_{TN})\sqrt{\frac{k_1}{k_1 + k_2}} \quad (12)$$

then transistor M_3 will be turned *on*, V_N starts to increase again, and the current I_o is diminishing. When V_o becomes equal to

$$V_{oC} = V_G + (V_G - V_{TN})\sqrt{k_1/k_3} \quad (13)$$

transistor M_2 will be completely turned off and I_o becomes equal to zero. At this instant, voltage V_N will be equal to $V_G - V_{TN}$ and M_1 is entering into saturation. Transistor M_1 carries the current

$$I_N = k_1(V_G - V_{TN})^2 \quad (14)$$

which is completely intercepted by M_3. Additional increase of V_o up to V_{DD} does not bring any changes and completes the current-voltage characteristic of the N-subcircuit.

Now the design problem can be formulated graphically [Fig. 2(c)]. Assuming that the trigger transition from one stable state to another takes place when the gate voltage has a required threshold value (say, V_H), and allowing a current ΔI to flow at this instant in the transistors M_1, M_2, M_3, and M_4, one has to find and superimpose the current-voltage characteristics of the two subcircuits so that only one unstable intersection point exists. A similar condition is then applied for another transition point, characterized by another required threshold voltage V_L. However, an attempt to obtain the device parameters from this direct approach gives an intractable system of nonlinear equations [the characteristics shown in Fig. 2(b) and (c) are simplifying approximations] and should be abandoned. Yet, the characteristics shown in Fig. 2(c) help to extend the approach [9] based on investigation of the trigger behavior near the transition point and to apply it to the circuit of Fig. 1(a). In addition, these characteristics allow provision of two inequalities useful in the trigger design. Finally, they help to clarify some details observed in the experimental transfer characteristics [1].

III. Thresholds, Transition, and Trigger Design

As mentioned earlier, the operation of the CMOS Schmitt trigger is known [1]. We will follow this description, modifying and interrupting it at appropriate points to obtain the results necessary for trigger design.

Assume that the voltage V_G in Fig. 1(a) is zero. Then transistors M_1 and M_2 are off. Transistors M_4 and M_6 are in the linear mode of operation, but the voltage drop at each is zero because the current in M_4 and M_5 is equal to the current in M_1 and M_2. The output voltage V_o is equal to V_{DD} (or *high*). Transistor M_3 is on (its drain and gate have the same voltage of V_{DD}) but it also does not carry any current.

When V_G rises above V_{TN}, transistor M_1 turns on and starts to conduct. The current of M_1 is determined by (14). It is completely intercepted by M_3, and the condition of the transistors in the P-subcircuit does not change. However, the potential V_N is starting to decrease.

The trigger operation starts when the voltage V_G arrives at the value of V_{Hi}. At this point, due to simultaneous increase of V_G and decrease of V_N, transistor M_2 turns on. It is not difficult to see that if in (13) one substitutes V_{DD} instead of V_{oC} (the gate of M_3 is still at V_{DD}) and V_{Hi} instead of V_G, one obtains the required relationship between the transistor parameters to start the triggering operation. It can be rewritten as

$$\frac{k_1}{k_3} = \left(\frac{V_{DD} - V_{Hi}}{V_{Hi} - V_{TN}}\right)^2. \quad (15)$$

By the same reasoning, one obtains that the condition

$$\frac{k_4}{k_6} = \left(\frac{V_{Li}}{V_{DD} - V_{Li} - |V_{TP}|}\right)^2 \quad (16)$$

should be satisfied to start the triggering operation when the input voltage becomes equal to V_{Li}.

The voltages V_{Hi} and V_{Li} are considered [1] as true thresholds of the CMOS Schmitt trigger. However, in effect, V_{Hi} and V_{Li} mark only the beginning of the triggering operation. The real triggering [Fig. 1(b)] occurs at close but different voltages V_H and V_L. The difference depends on choice of the parameters k_2 and k_5, and can be estimated as follows.

The transition from one stable state to another in the Schmitt trigger is, indeed, very fast, and one can consider that during it the trigger input voltage does not change and stays at V_H for the considered transition of the output voltage from *high* to *low*. When M_2 is turned on, the trigger starts to operate as a linear circuit with positive feedback. Transistors M_4 and M_5 are, in accordance with the P-subcircuit voltage-current characteristic, in a linear mode of operation, and the trigger can be represented as the linear circuit shown in Fig. 3(a). Transistor M_1 carries the current

$$I_{NH} = k_1(V_H - V_{TN})^2 \approx k_1(V_{Hi} - V_{TN})^2. \quad (17)$$

The trigger load is

$$R_{LP} = \frac{k_4^{-1} + k_5^{-1}}{2(V_{DD} - V_{Hi} - |V_{TP}|)} \quad (18)$$

which is analogous to (6). The small-signal model for this part of trigger operation is shown in Fig. 3(b). The loop-transfer function for this circuit is

$$A_L = \frac{g_{m3}R_{LP}(g_{m2}r_{o1} + 1)}{(g_{m2} + g_{m3})r_{o1} + 1}. \quad (19)$$

Here r_{o1} is the output impedance of M_1, which, as follows from the previous operation, is operating in the saturation region. At the instant of the output voltage jump from *high* to *low*, this loop–transfer

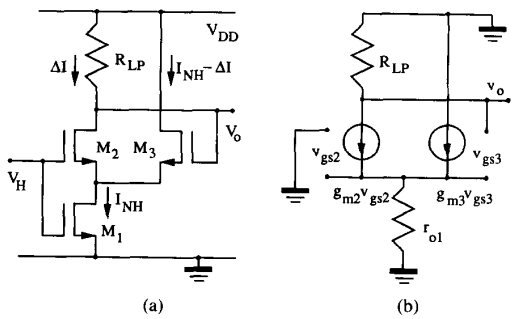

Fig. 3. CMOS Schmitt trigger during transition: (a) equivalent circuit and (b) small-signal model.

function becomes equal to unity. Assuming $g_{m2}r_{o1} \gg 1$ (which is usually satisfied), this gives the condition of transition

$$\frac{R_{LP}}{g_{m2}^{-1} + g_{m3}^{-1} + (r_{o1}g_{m2}g_{m3})^{-1}} = 1. \tag{20}$$

The current of M_1 at this instant is divided between M_2 and M_3 into two parts ΔI and $I_{NH} - \Delta I$ so that the transconductance of the corresponding transistors are

$$g_{m2} = 2\sqrt{\Delta I k_2} \tag{21}$$

and

$$g_{m3} = 2\sqrt{(I_{NH} - \Delta I)k_3} \approx 2\sqrt{I_{NH}k_3}. \tag{22}$$

The analysis shows that the last term in the denominator of (20) can be discarded as well and one can use the simplified transition condition

$$g_{m2}^{-1} + g_{m3}^{-1} \approx R_{LP}. \tag{23}$$

If (21) and (22) are substituted in (23), and (17) and (18) are used as well, then

$$\Delta I = k_2^{-1}\left[\frac{k_4^{-1} + k_5^{-1}}{V_{DD} - V_{Hi} - |V_{TP}|} - \frac{1}{(V_{Hi} - V_{TN})\sqrt{k_1 k_3}}\right]^{-2}. \tag{24}$$

This value depends on k_2 and k_5. It allows one to estimate the difference between V_H and V_{Hi}. Indeed, when the transition starts one has the input voltage of V_{Hi}, transistor M_2 has zero current, transistor M_3 carries the current of I_{NH}, and the trigger output voltage is equal to V_{DD}. Just before the output voltage jump, one has the input voltage of V_H, transistor M_2 has the current of ΔI, M_3 carries the current of $I_{NH} - \Delta I$, and the output voltage drops to $V_{DD} - \Delta I R_{LP}$. Using these conditions, it is easy to find that

$$\Delta V_H = V_H - V_{Hi} \approx \sqrt{\frac{\Delta I}{k_2}} - \Delta I R_{LP}. \tag{25}$$

If transistor M_3 is very wide one can use the approximation

$$\Delta I \approx \frac{(V_{DD} - V_{Hi} - |V_{TP}|)^2}{k_2(k_4^{-1} + k_5^{-1})^2}. \tag{26}$$

Then, if in (25) the term $\Delta I R_{LP}$ is neglected [indeed, it should be much less than $|V_{oS}|$ for the P-subcircuit, otherwise the model of Fig. 3(a) is not valid] and (26) is substituted in (25), one obtains

$$\Delta V_H \approx \frac{V_{DD} - V_{Hi} - |V_{TP}|}{\frac{k_2}{k_5} + \frac{k_2}{k_4}}. \tag{27}$$

Similarly, considering the transition of the output voltage from low to high, one finds that

$$\Delta V_L = V_L - V_{Li} \approx -\frac{V_{Li} - V_{TN}}{\frac{k_5}{k_2} + \frac{k_5}{k_1}}. \tag{28}$$

The values given by (27) and (28) can be considered as the worst case deflections of the thresholds. It is seen from (27) and (28) that, to reduce ΔV_H and $|\Delta V_L|$, the ratio k_2/k_5 should be kept constant and each of k_2/k_4 and k_5/k_1 should be increased simultaneously.

Equations (17) and (18) together with (27) and (28) provide necessary information for the CMOS Schmitt trigger design. The exact values V_H and V_L of the threshold voltages are of paramount importance in all multivibrator applications of Schmitt triggers [11]–[13].

In the design practice, it is difficult to achieve P- and N- subcircuits with the shape of their voltage-current characteristics, as shown in Fig. 2(c) (for a given V_G voltage). Usually (to reduce the value of ΔI for less power dissipation at high-frequency operation) one of them has the shape shown by the dotted line. In this case, one obtains the second stable intersection point of the voltage-current characteristics, and the output voltage after transition drops to V_{oL} (in the opposite transition it will go to V_{oH}). This results in the experimentally observed [1] "tails" of the transfer characteristics [Fig. 1(b)]. The output voltage arrives to zero value when the voltage V_G becomes close to the value of $V_{DD} - |V_{TP}|$ (in the opposite transition it arrives to V_{DD} when V_G drops below V_{TN}). To make the transfer characteristic more rectangular and reduce the tails (fortunately, one simultaneously reduces ΔI as well), the condition [Fig. 2(c)]

$$I_{oPH} \ll I_{oNH} \tag{29}$$

should be satisfied for the transition from high to low. The current I_{oNH} in (29) can be calculated using (11) and V_H as V_G. This gives

$$I_{oNH} \approx \left(\frac{k_1 k_2}{k_1 + k_2}\right)(V_H - V_{TN})^2 \tag{30}$$

and, in a similar way,

$$I_{oPH} \approx \left(\frac{k_5 k_4}{k_5 + k_4}\right)(V_{DD} - V_H - |V_{TP}|)^2. \tag{31}$$

Of course, near another transition point, the condition

$$I_{oPL} \gg I_{oNL} \tag{32}$$

should be satisfied. Here

$$I_{oPL} \approx \left(\frac{k_5 k_4}{k_5 + k_4}\right)(V_{DD} - V_L - |V_{TP}|)^2 \tag{33}$$

and

$$I_{oNL} \approx \left(\frac{k_1 k_2}{k_1 + k_2}\right)(V_L - V_{TN})^2. \tag{34}$$

Conditions (29) and (32) are easily satisfied for the triggers with a wide loop of the transfer characteristic. However, it is difficult to satisfy them in the triggers of a narrow hysteresis loop.

IV. Example

Assume that it is required to design a Schmitt trigger with the threshold values of $V_{Hi} = 3.8$ V and $V_{Li} = 1.8$ V. The circuit should operate with $V_{DD} = 5$ V. The circuit is realized in the CMOS process with device transconductance parameters of $(\mu_n C_{ox})/2 = 16.2\ \mu A/V^2$ and $(\mu_p C_{ox})/2 = 7.2\ \mu A/V^2$. The device threshold voltages are $V_{TN} = 0.55$ V and $|V_{TP}| = 0.60$ V (these process parameters are typical for SACMOS 3-μ m process technology [14], and the example under discussion was designed as part of a humidity-sensitive multivibrator realized in this technology).

Substituting the values of V_{DD}, V_{Hi}, and V_{TN} in (16), one finds that $k_3/k_1 = 7.33$. If one takes $(W/L)_1 = (6/6)$, where both the width and length are in microns, then one has to choose the closest rounded values of $(W/L)_3 = (44/6)$. Notice that it is impossible

to choose the device M_3 of minimal geometry, as is suggested in [1]. The chosen device geometries give $k_1 = 16.2\ \mu A/V^2$ and $k_3 = 118.8\ \mu A/V^2$.

Using the values of V_{DD}, V_{Li}, and $|V_{TP}|$ one obtains from (17) that $k_6/k_4 = 2.09$. If one takes $(W/L)_4 = (14/6)$ (this gives $k_4 = 16.8\ \mu A/V^2$) then $k_6 = 35.1\ \mu A/V^2$ and $(W/L)_6 = (29/6)$.

If one takes $k_2 = 3k_1 = 48.6\ \mu A/V^2$ and $k_5 = 5k_4 = 84\ \mu A/V^2$ then one can take, for example, $(W/L)_2 = (18/6)$ and $(W/L)_6 = (70/6)$. Using the previously chosen device parameter values, one finds from (27) and (28) that $\Delta V_H = 0.17$ V and $\Delta V_L = -0.18$ V. Thus the trigger changes states at $V_H = 3.97$ V and $V_L = 1.62$ V, the values that are different from V_{Hi} and V_{Li}. The difference can be reduced if the width of the devices is increased. These results were verified using the ESPICE [15] simulation program and were observed later in experimental circuits.

Finally, one can find from (30) and (31) that $I_{oNH} = 142.1\ \mu A$ and $I_{opH} = 2.6\ \mu A$. Thus, (29) is satisfied. Similar calculations using (33) and (34) give $I_{oPL} = 108.2\ \mu A$ and $I_{oNL} = 13.9\ \mu A$ and (32) is, hence, satisfied as well. The difference between I_{oPL} and I_{oNL} allows to see in simulations a small "tail" after the transition from low to high.

V. Conclusions and Discussion

The design of a CMOS Schmitt trigger can be completed if the detailed circuit operation near the transition points is analyzed. This analysis gives true thresholds and allows one to evaluate the difference between the thresholds and the initial points of transitions (which are incorrectly considered and specified as thresholds). The voltage-current characteristics of the trigger subcircuits allow one to specify the conditions to make the trigger transfer characteristic more rectangular. The analysis is valid if the fabrication technology allows using the square-law characteristics of MOS devices.

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An Analytical Model for the Transient Response of CMOS Class *AB* Operational Amplifiers

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***Abstract*—An analytical study of the transient response of a CMOS class *AB* opamp operating in a voltage follower configuration is presented. As with class *A* opamps, we identify nonlinear and linear regions of operation corresponding to slewing and settling periods in the transient response. But in contrast with class *A* opamps, it is shown that the feedback configuration should be considered for the entire duration of the transient response. It is shown that doublets (pole-zero pairs) have significant impact on the transient response of the class *AB* opamps in both nonlinear and linear regions of operation. One result is that in order to prevent overshoot in the transient response due to the doublets, the pole of the double should be located at a frequency higher than about four times the unity–gain bandwidth. The proposed analytical model is valid for any location of the doublets. It agrees well with the results of HSPICE computer simulations, and has the advantage over the latter of providing circuit designers with a clear relationship between the design goals and the device parameters.**

I. Introduction

The period of time in which an opamp settles to a given percentage of the output voltage is one of its most important features. It consists of slewing and settling periods [1]. The minimization of each is necessary in order to achieve the optimal transient response. The slewing of an opamp is associated with its nonlinearities. In class A opamps, it is due to the limited supply of current to charge a compensation capacitor. The main feature of a class AB opamp, such as the one shown in Fig. 1, is the ability to deliver a large output current during the transient [2], thus reducing slewing. For example, Castello and Gray analyzed a class AB opamp, whose output current changes 45 times from 2 μA in the steady-state to 90 μA peak value during the transient [3]. Nevertheless, class AB opamps exhibit slewing. This is because the drastic variations in the current during the transient are associated with nonlinearities of MOSFET's. In this paper, we investigate analytically the transient response of class AB opamps during the slewing and settling periods. We show that doublets (pole-zero pairs) affect the transient response significantly in the both periods. The effect of doublets in class A bipolar opamps was shown by Kamath *et al.* to degrade amplifier performance [1]. Kamath *et al.* have not discussed, however, the effect of doublets on the slewing period. But our earlier simulations of class AB opamps have shown that as a result of changing the doublet parameters, the shape of the voltage transient response during the slewing period is significantly modified [4]. Furthermore, the analysis by Kamath *et al.* was limited to the case of a closely spaced doublet inside the unity–gain bandwidth (UGB). This assumption is justified for bipolar opamps, in which doublets appear at low frequencies as a result of capacitive bypass of lateral p–n–p transistors having poor frequency response [5]. In CMOS class AB opamps, doublets are caused by the level shifters that are biasing the input stage (see Fig. 1). In CMOS technology, the frequency response of the level shifters can be changed by altering the biasing current and geometry of MOS

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