Frequency Dividers

Professor Jri Lee

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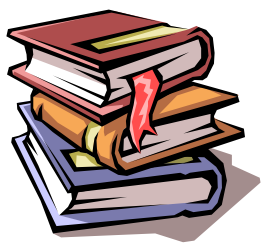
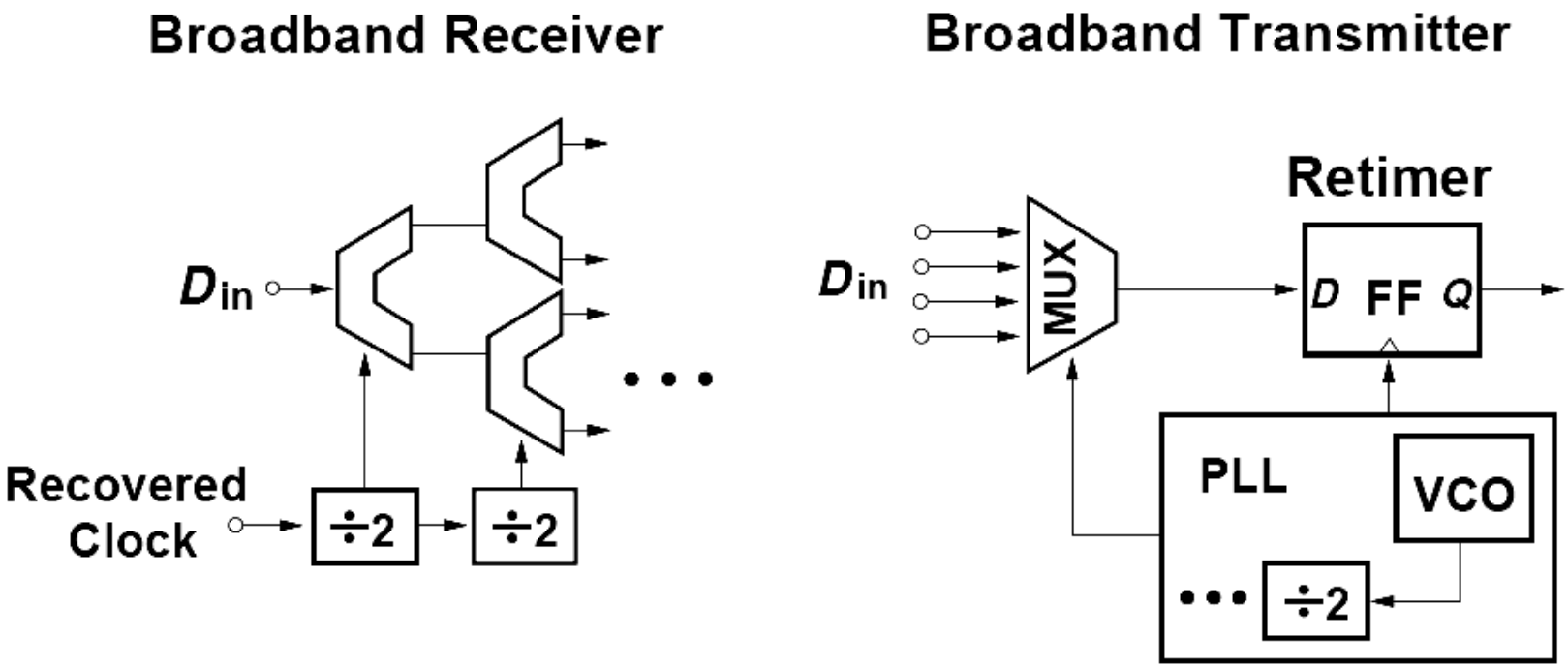


Electrical Engineering Department
National Taiwan University

Outline

- Introduction
- Static Dividers
- Miller Dividers
- Injection Dividers
- Prescalers
- Case Study

Full-Rate Divider Applications



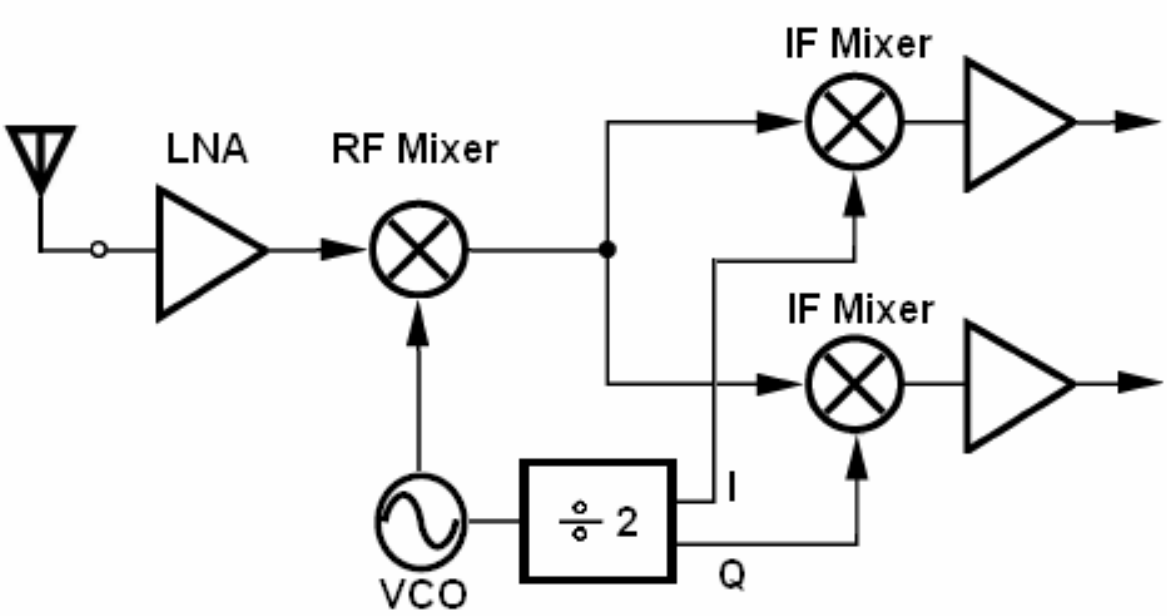
- Half−rate retimer in transmitter would be prone to clock and device asymmetries

  => Must use a full−rate retimer.

  => Need a 40−GHz divider.

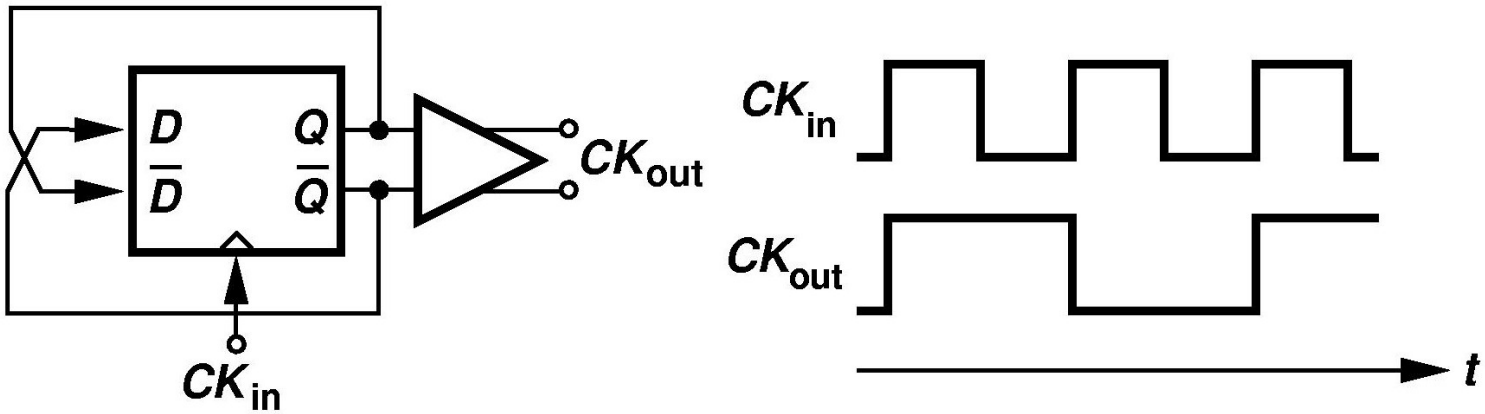
Full-Rate Divider Applications

Wireless Frontend



- I/Q mismatch of great importance.
- Very high speed.

Static Dividers

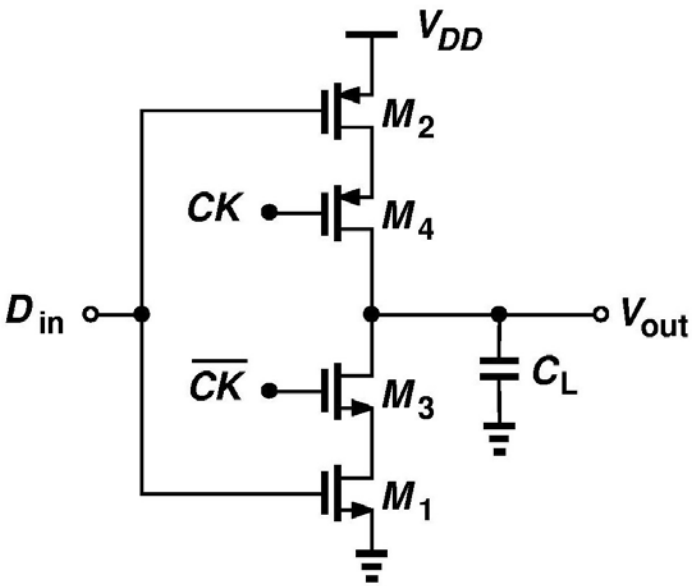


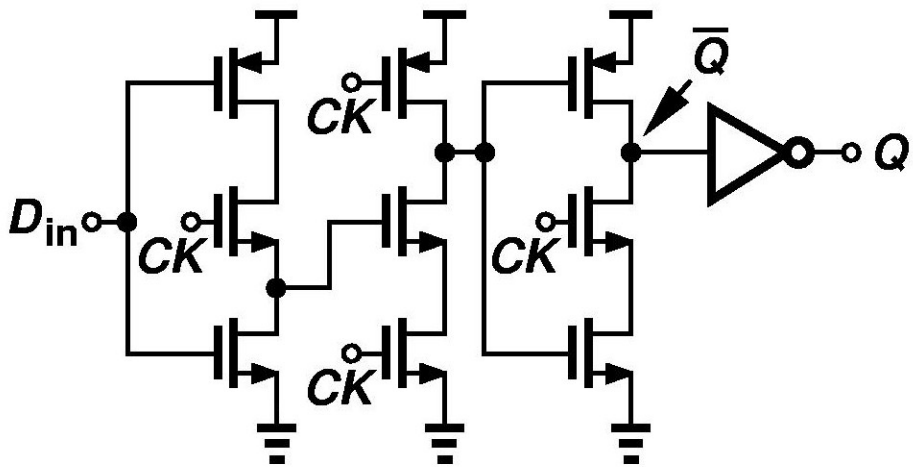
- Edge-triggered flipflop toggle between the two states by “negative feedback”.
- Wide range of operation (almost from DC to the circuit’s bandwidth).
- Overlapped clock may cause racing.

  ⇨ Rising/falling time of CK_{in} matters.

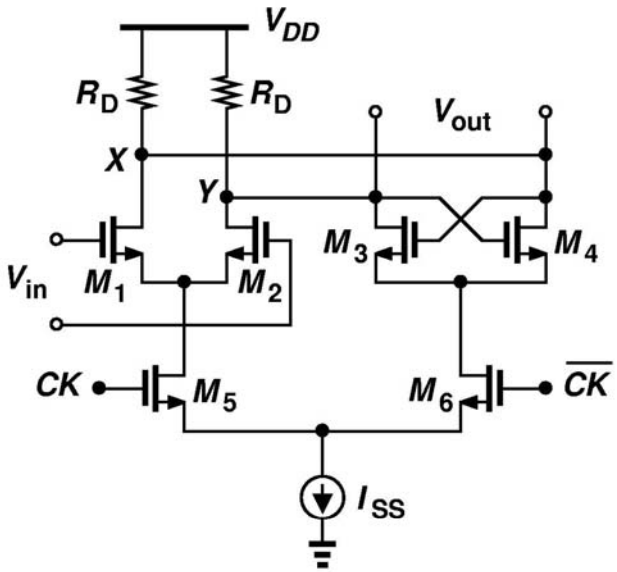
Implementation of Flipflops

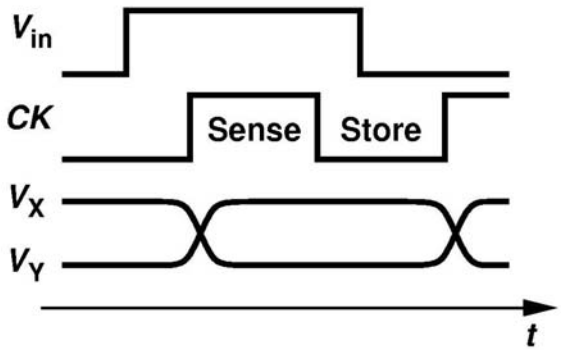
- **Almost any type (digital or analog) can serve:**
  - **Multiplexer-Based**
  - **Pseudostatic**
  - **C²MOS**
  - **TSPC**
  - **CML (Current-Steering)**

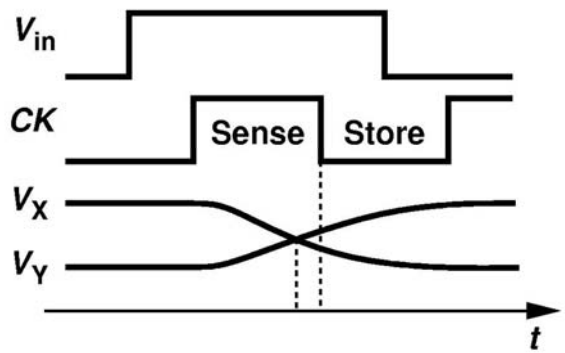




CML Latch

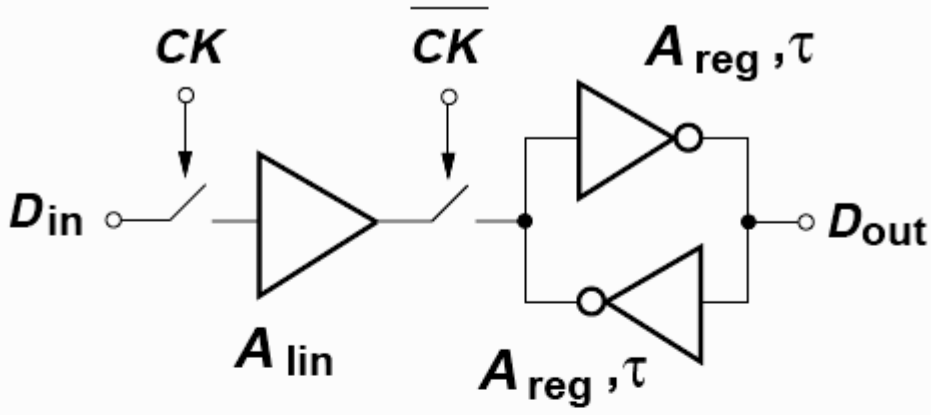






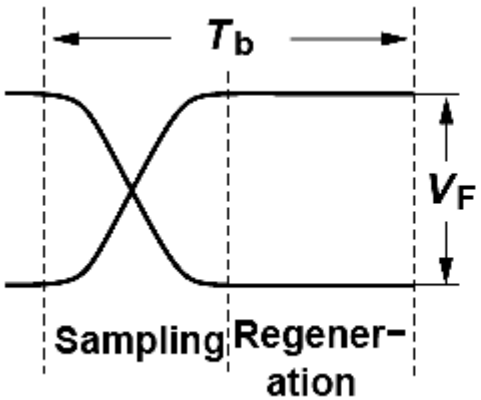
- **Speed limited by *RC* time constant.**

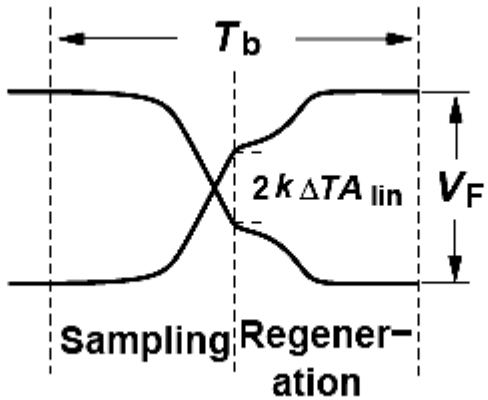
Meta-Stability

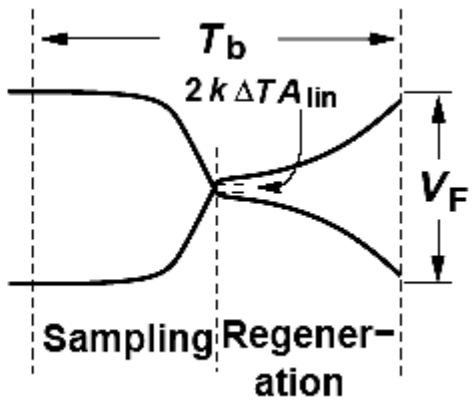


- Metastable sampling may cause incomplete regeneration, leading to a finite slope at small $\Delta\phi$.
- Depends on linear gain A_{lin}, regeneration gain A_{reg}, and time constant τ.

Regeneration of Meta-Stable Points

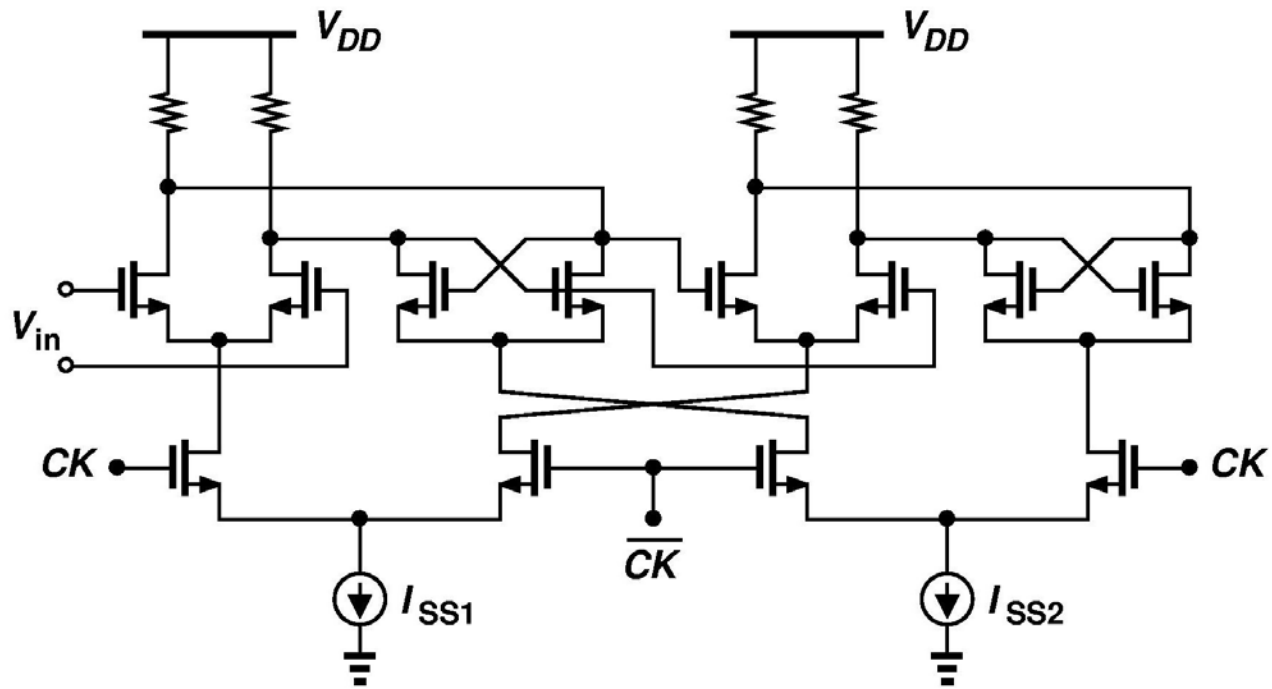






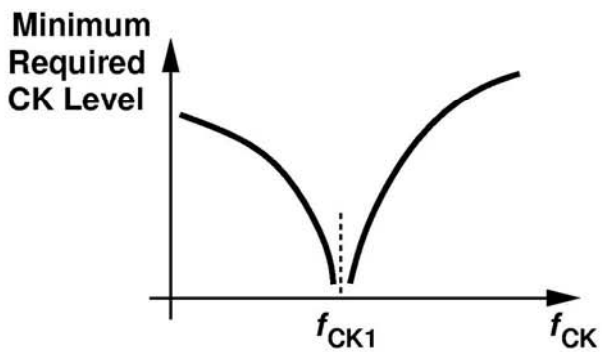
- **FF-based divider fails when it can not flip the state in one (input) clock cycle.**

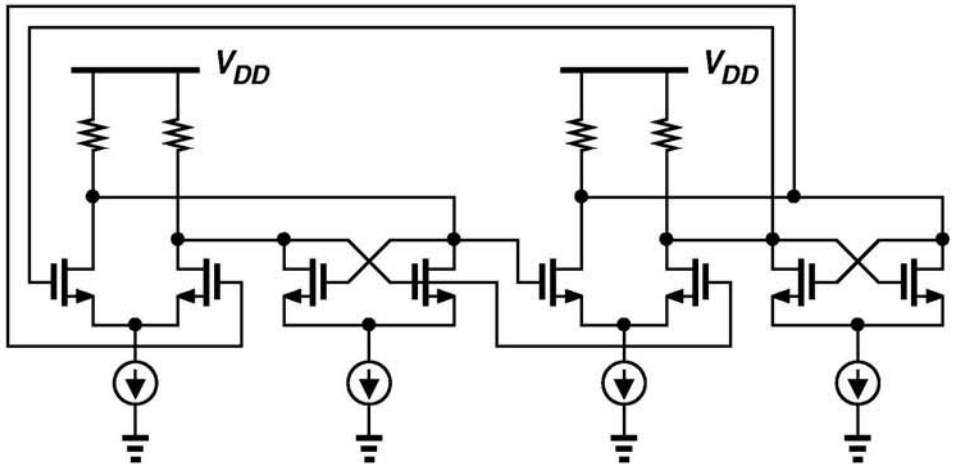
Superdynamic Flipflop



- Allows different current for sampling and regeneration.

Free-Running Frequency

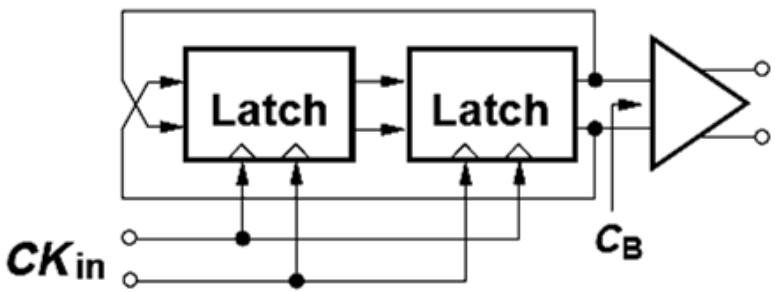




- At f_{CK1} the divider behaves as a ring oscillator (with the cross-coupled pair providing sufficient phase shift), and requires little input power.

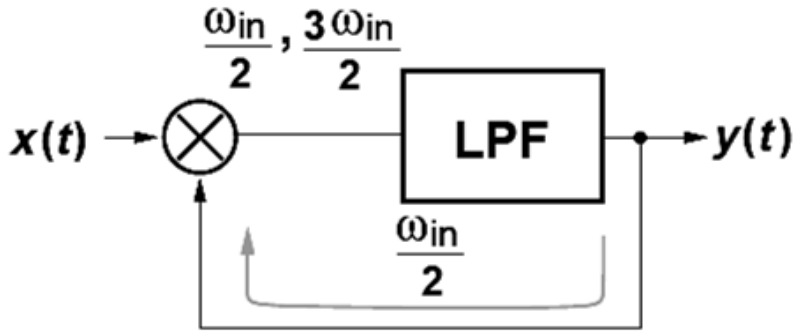
Static and Dynamic Dividers

Static Divider



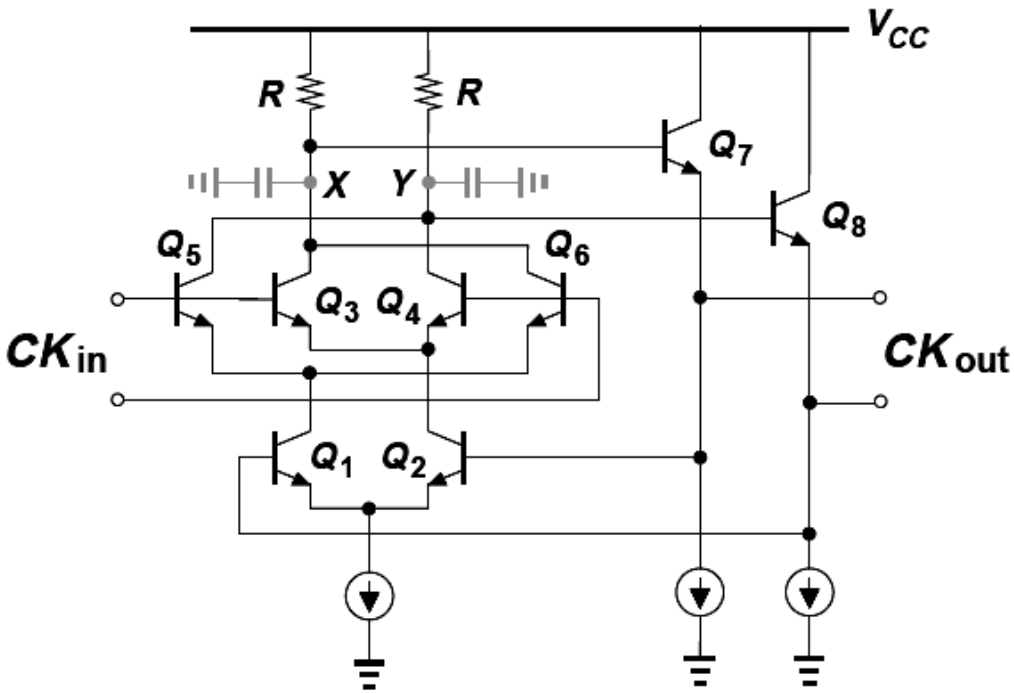
- Buffer input capacitance degrades the speed considerably.
- Speed limited to 18 GHz in 0.18−μm CMOS Technology.

Dynamic (Miller) Divider



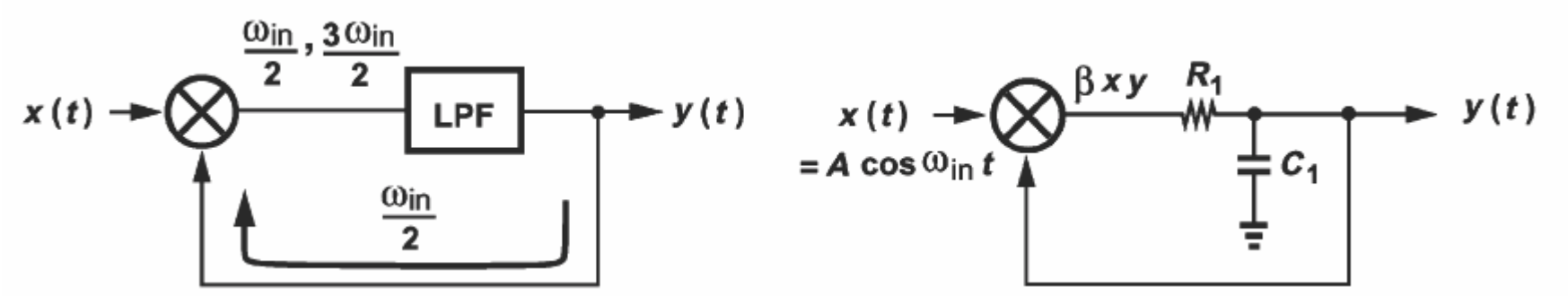
- LPF absorbs circuit parasitics => High−speed operation.
- Circuit must satisfy certain phase shift requirements.

Conventional Dynamic Divider



- Exploits natural low−pass filtering at *X* and *Y*.
- Devices in the loop contribute enough phase shift for startup.
- But load resistance would consume large voltage headroom in CMOS.

Analysis of Dynamic (Miller) Divider

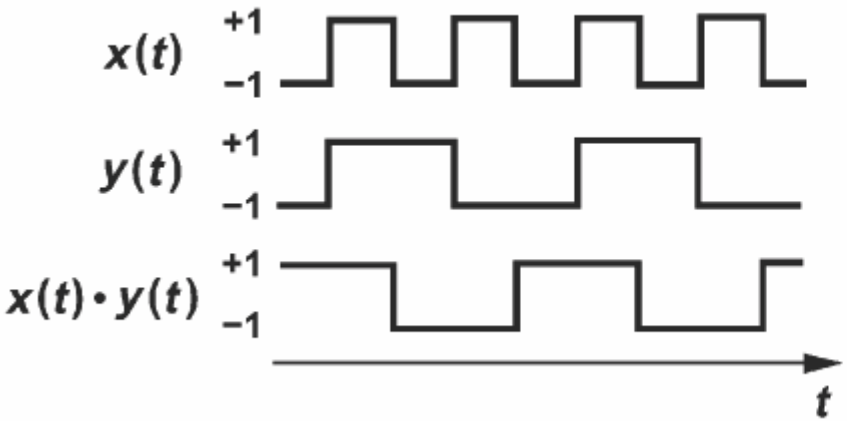


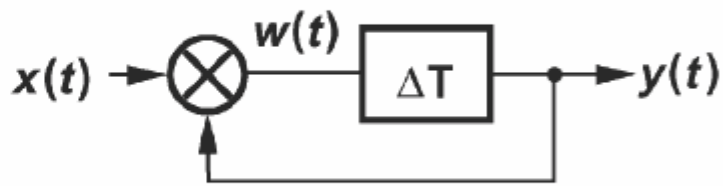
$$R_1C_1\frac{dy}{dt} + y = \beta yA\cos\omega_{in}t$$

$$\Rightarrow\ y(t) = y(0)\exp\left(-\frac{t}{R_1C_1} + \frac{\beta A}{R_1C_1\omega_{in}}\sin\omega_{in}t\right)$$

- Decays to zero with a time constant of R_1C_1.
- Divider doesn't work without proper delay along the loop.

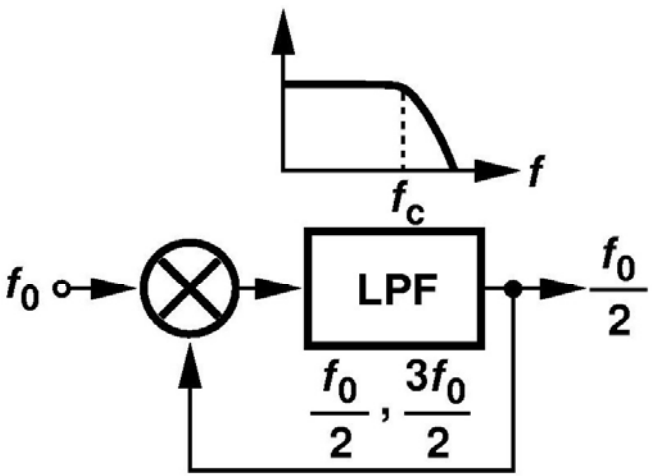
Analysis of Dynamic Divider

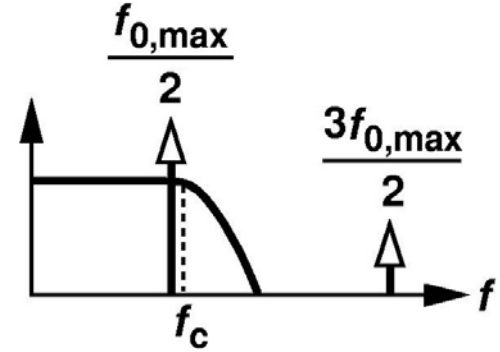


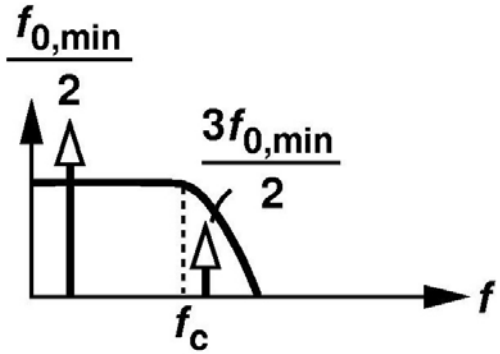


- 90° phase shift satisfies the division requirement.
- Usually an emitter follower is needed to provide the required phase shift.

Rough Estimation of Operation Range





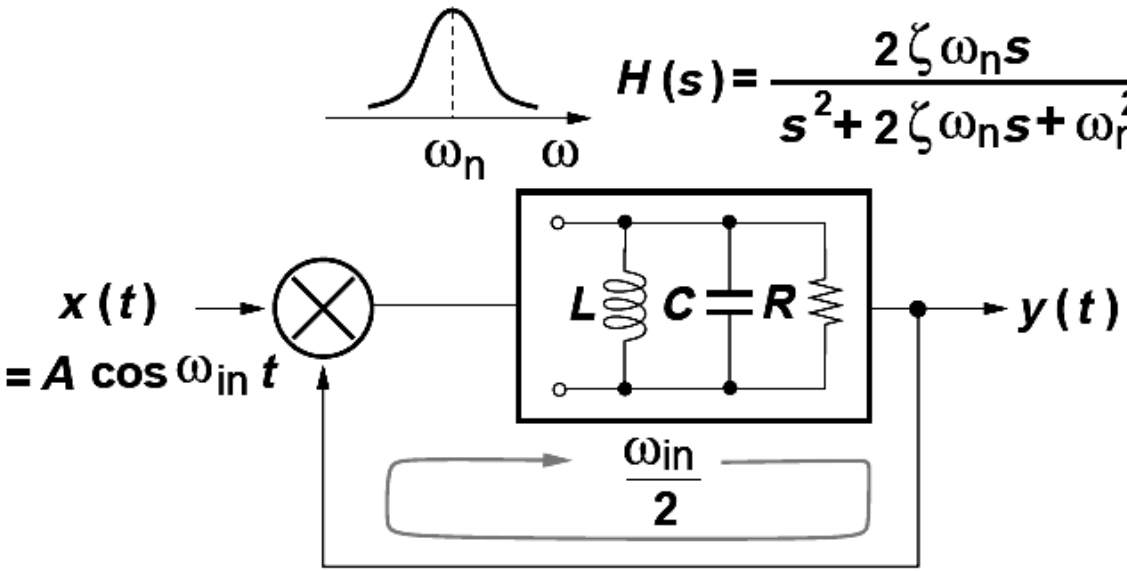


- The LPF must (1) filter out $\frac{3f_0}{2}$, (2) preserve $\frac{f_0}{2}$.

⇨ $\frac{f_{0,max}}{2} \cong f_c$ and $\frac{3f_{0,min}}{2} \cong f_c$

⇨ $\frac{2f_c}{3} < f_0 < 2f_c$

Dynamic Divider with Bandpass Load



Loop gain requirement:

$$\frac{\beta A}{2} \left| H\left(j \frac{\omega_{in}}{2}\right) \right| \geq 1$$

Thus,

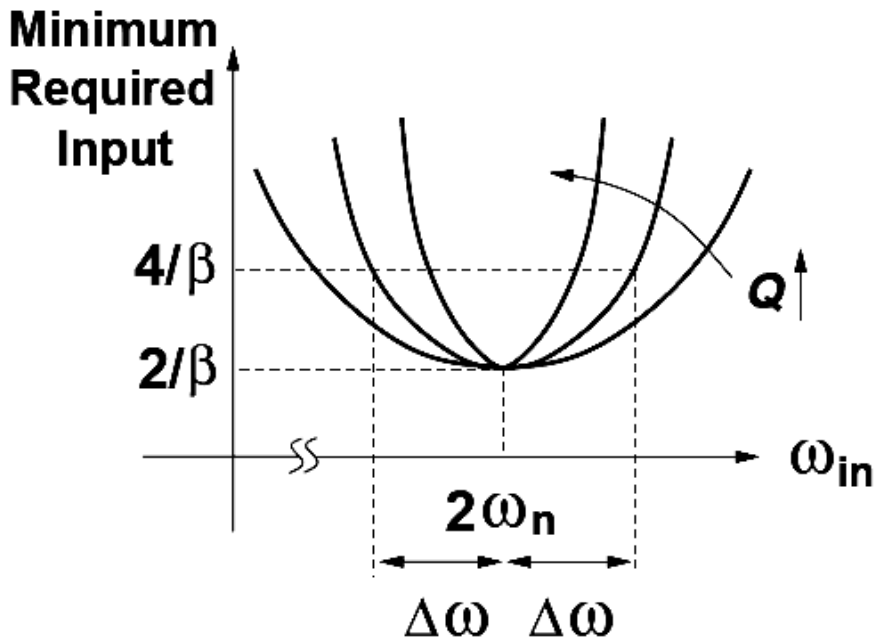
$$A \geq \frac{2}{\beta} \sqrt{1 + \frac{\left(1 - \frac{\omega_{in}^2}{4\omega_n^2}\right)^2}{\zeta^2 \frac{\omega_{in}^2}{\omega_n^2}}}$$

Frequency Range for Correct Division

$$A \geq \frac{2}{\beta}\sqrt{1+\frac{\left(1-\frac{\omega_{in}^2}{4\omega_n^2}\right)^2}{\zeta^2\frac{\omega_{in}^2}{\omega_n^2}}}$$

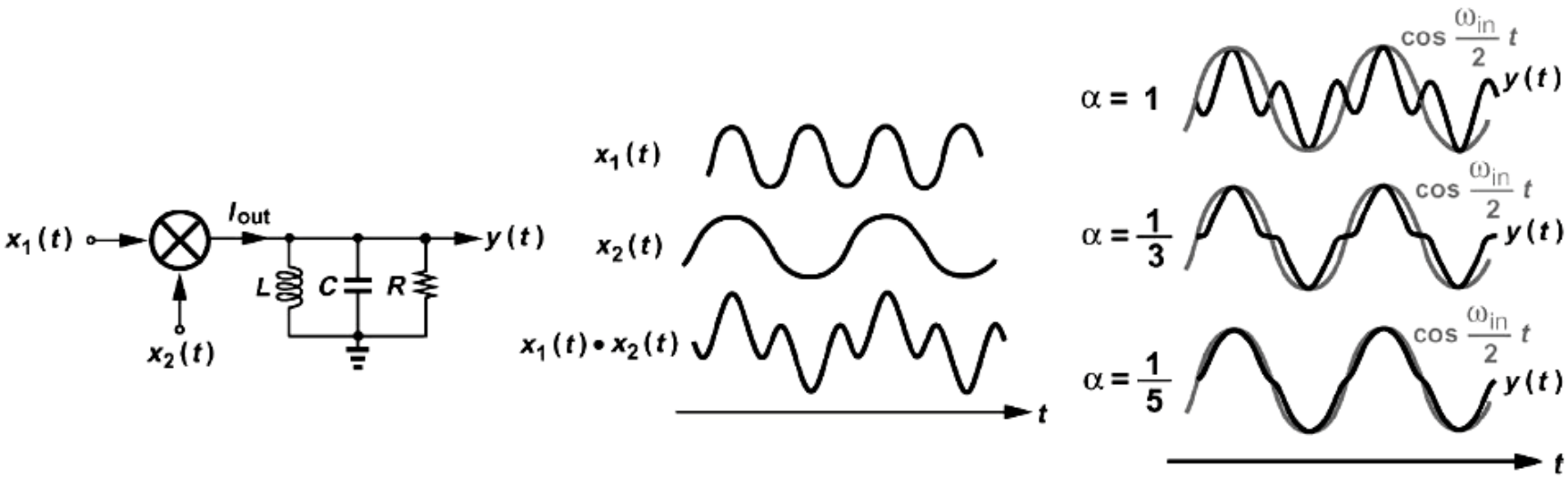
for $\Delta\omega = |\omega_{in} - 2\omega_n| << 2\omega_n$:

$$A \geq \frac{2}{\beta}\sqrt{1+\left(\frac{Q\Delta\omega}{\omega_n}\right)^2}$$



For Example, if $A_{max} = \frac{4}{\beta}$, $\Delta\omega = \frac{\sqrt{3}}{Q}\omega_n$

Intuitive Understanding of Bandpass Division

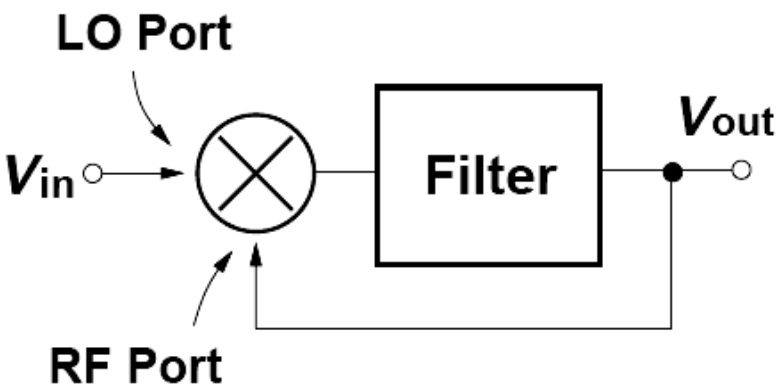


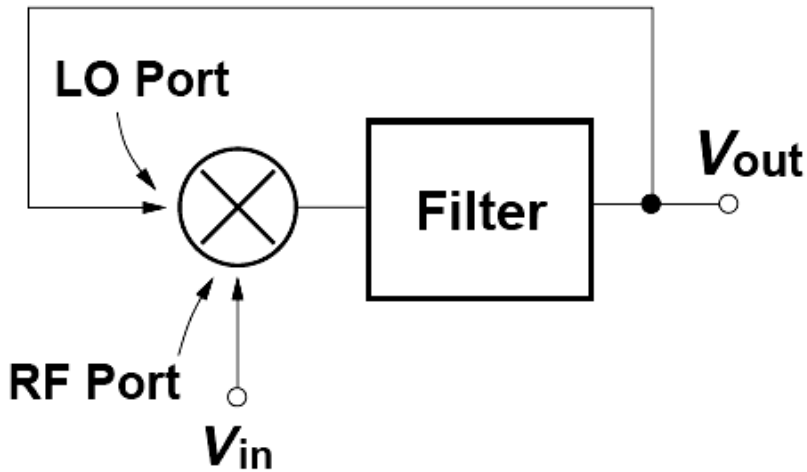
$$y \propto \cos\frac{\omega_{in}t}{2} + \alpha\cos\frac{3\omega_{in}t}{2} \qquad \Rightarrow 0 < \alpha < 1/3.$$

Actually, $\Rightarrow 0 < \alpha < 1/(2\sqrt{3})$.

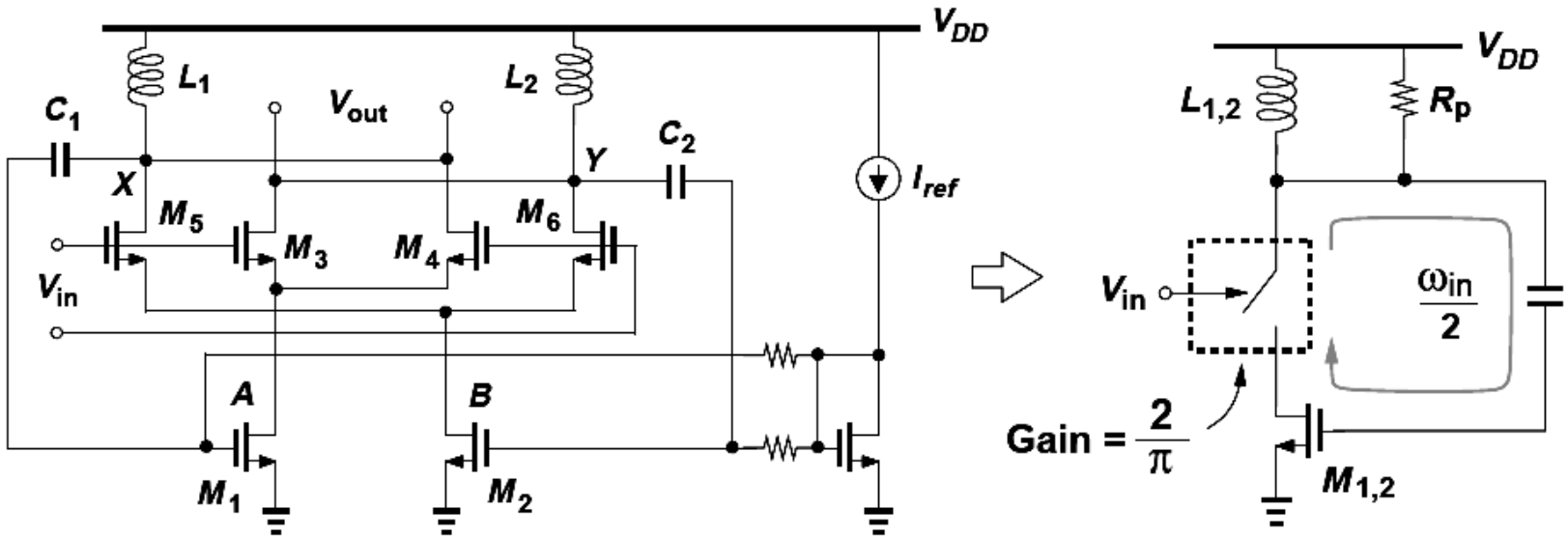
Reference: "A 40-GHz Frequency Divider in 0.18-um CMOS Technology", JSSC, April 2004.

RF-Port and LO-Port Feedback





RF-Port Feedback



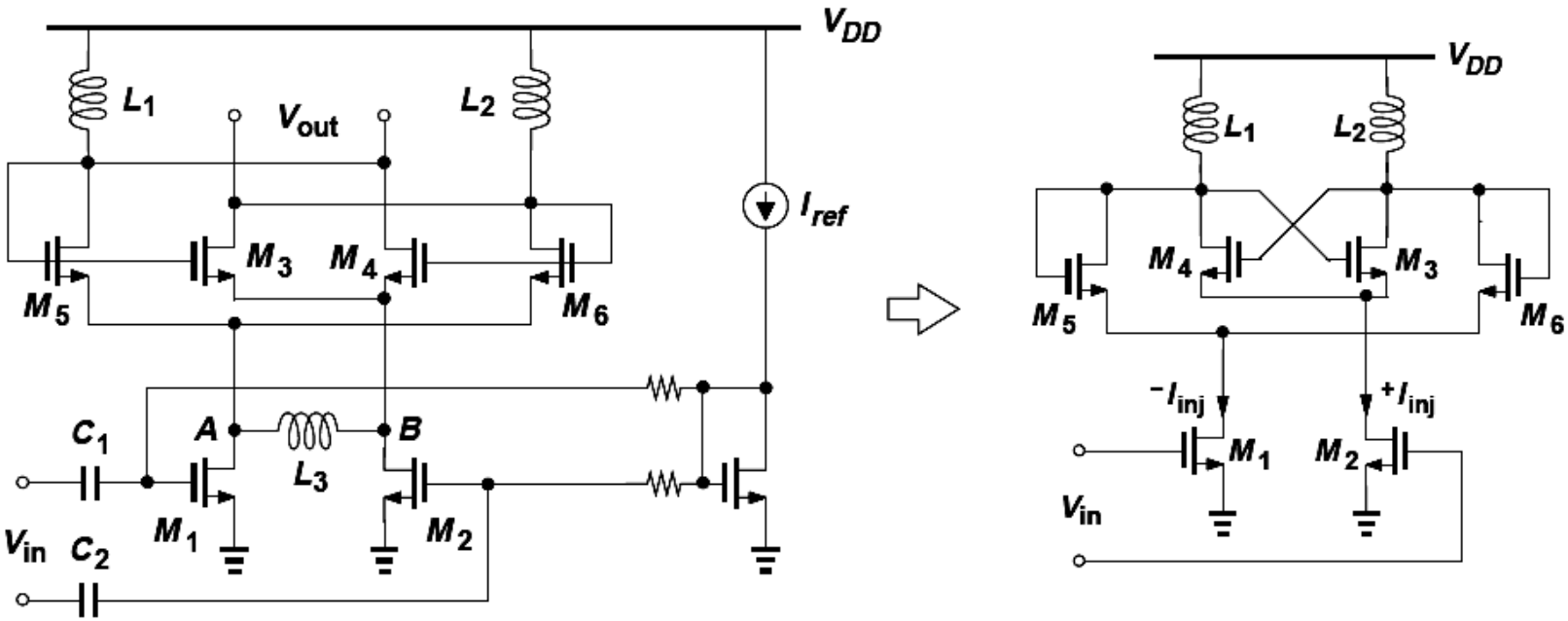
Nonidealities:

- Current Loss at A and B
- Gradual Switching of $M_3 - M_6$
- Parasitics at X and Y

$$\text{Loop gain} = \frac{2}{\pi} g_{m1,2} R_p$$

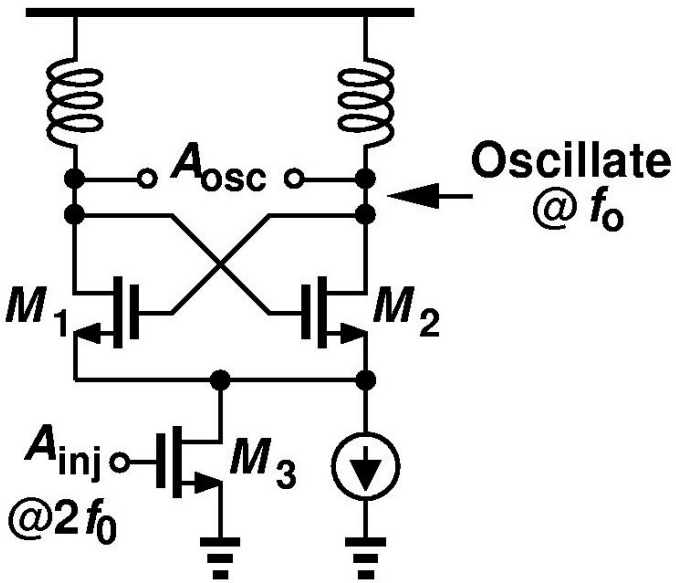
$$\begin{cases} R_p = Q L_{1,2} \dfrac{\omega_{in}}{2} \\ g_m = 2\pi f_T C_{GS} \\ \dfrac{\omega_{in}}{2} = \dfrac{3}{\sqrt{C_{GS} L_{1,2}}} \end{cases} \Rightarrow Q = \frac{\pi}{2} \cdot \frac{f_{in}/2}{f_T}$$

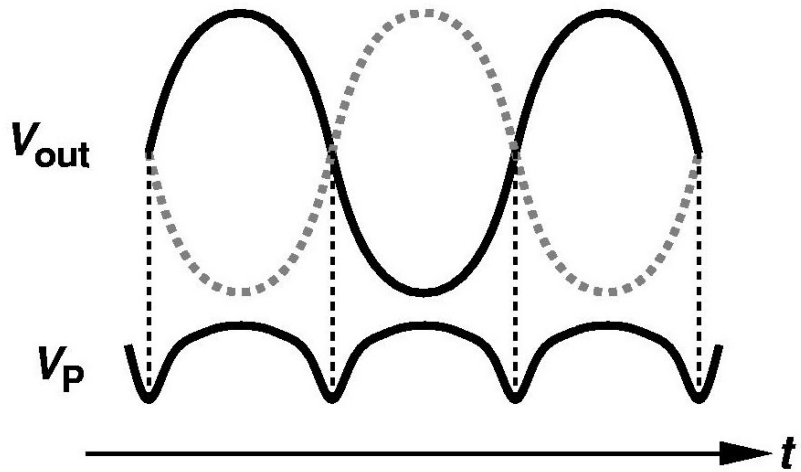
LO-Port Feedback



- With feedback applied to LO port, the circuit resembles an injection−locked divider.

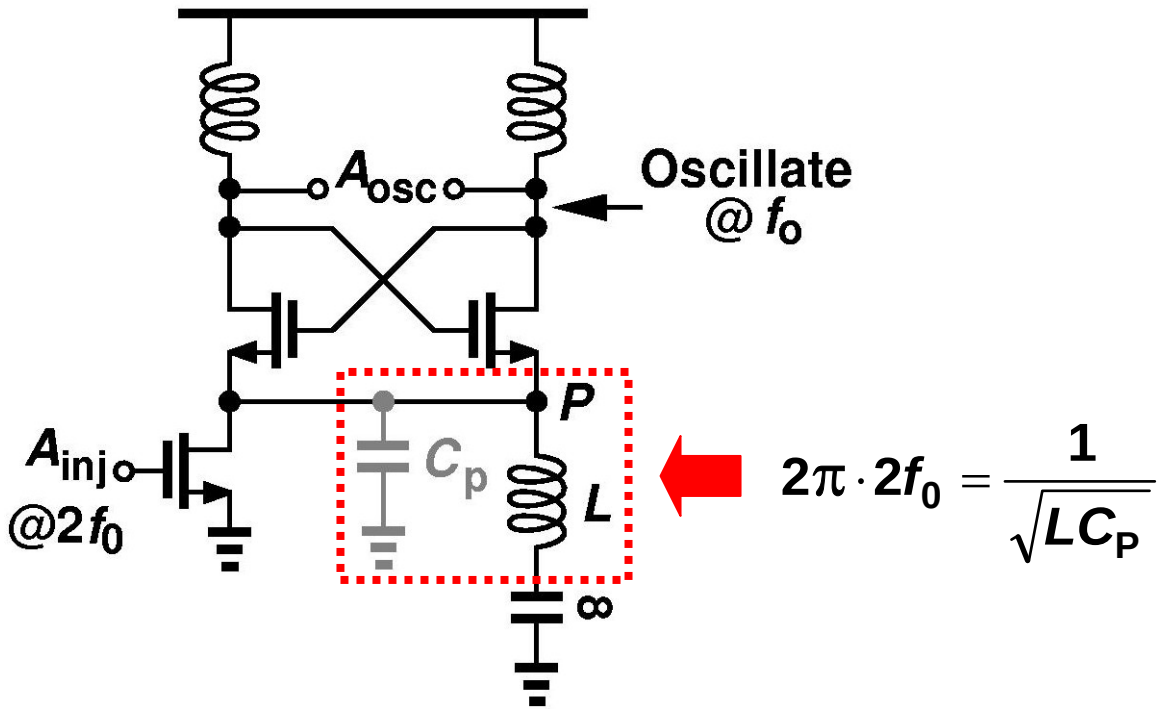
Injection-Locked Divider





- Injecting signal at twice the oscillation frequency.
- Locking range $\cong \frac{f_0}{2Q} \cdot \frac{A_{inj}}{A_{osc}} \cdot \frac{4}{3\pi}$

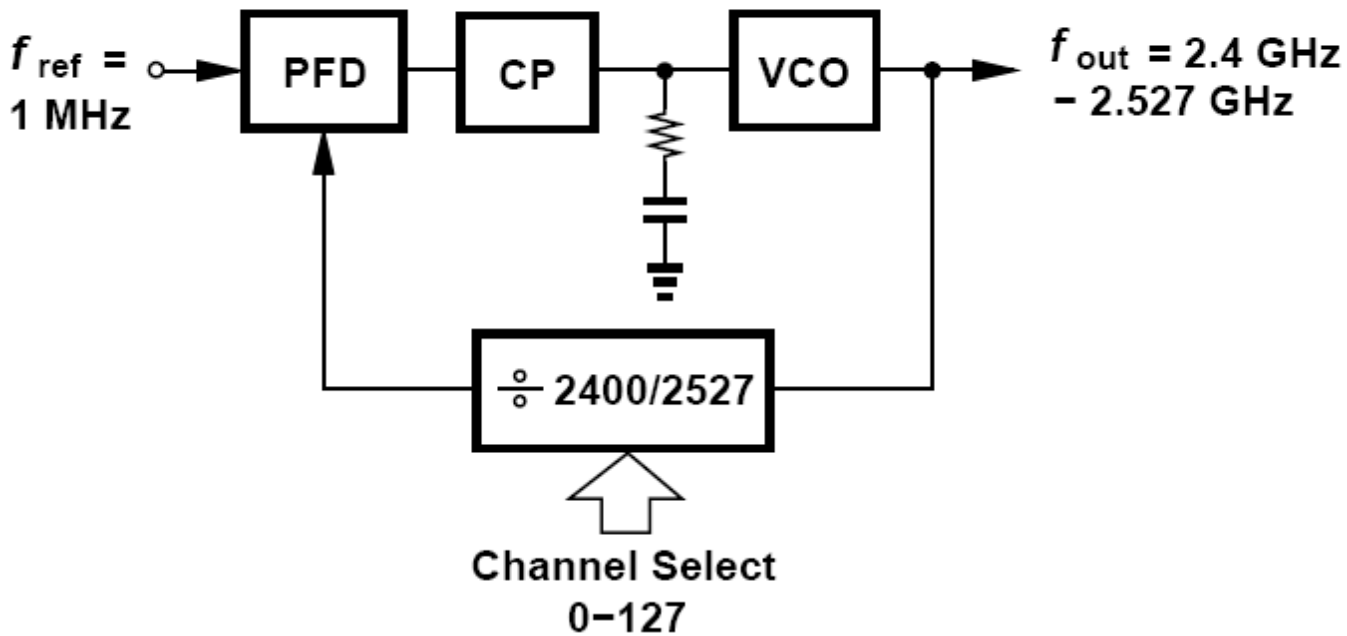
Modified Injection-Locked Divider



- Resonate out parasitic capacitance at node *P* to allow stronger signal injection to the divider.

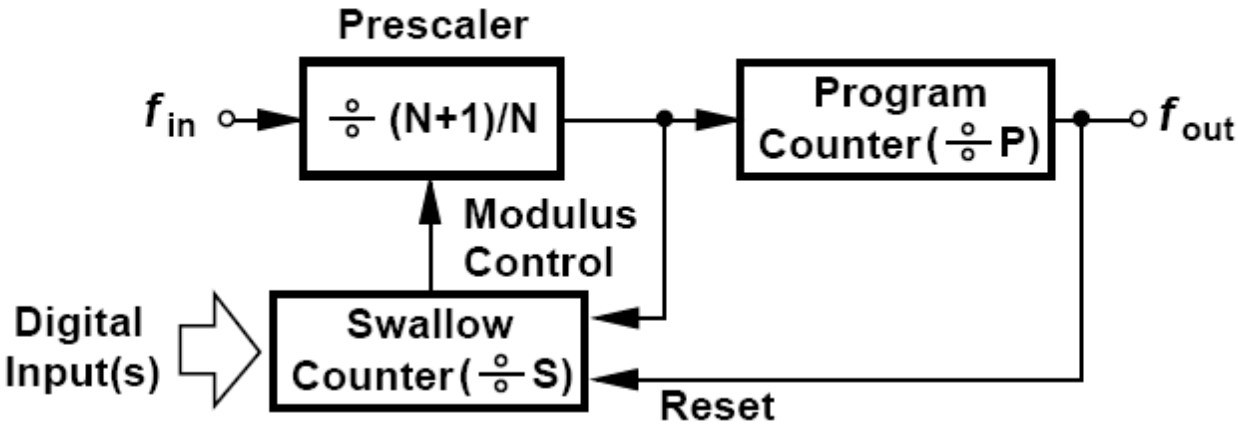
Multi-Modulus Divider

- Some applications require programmable division.
- Example: Integer-N Frequency Synthesizer.



Channel Spacing = 1 MHz, Channel Number = 128

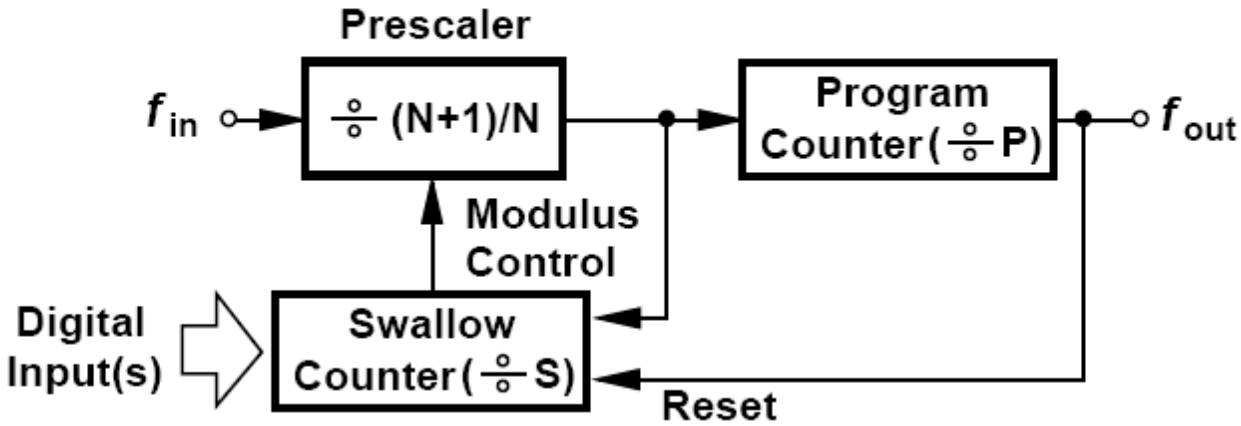
Pulse-Swallow Divider



$$f_{out} = \frac{f_{in}}{NP+S}$$

- Prescaler divides the input frequency by N + 1 or N based on the modulus control.
- Program counter divides the prescaler output by P (fixed).
- Swallow counter divides the prescaler output by S (programmable).

Pulse-Swallow Divider



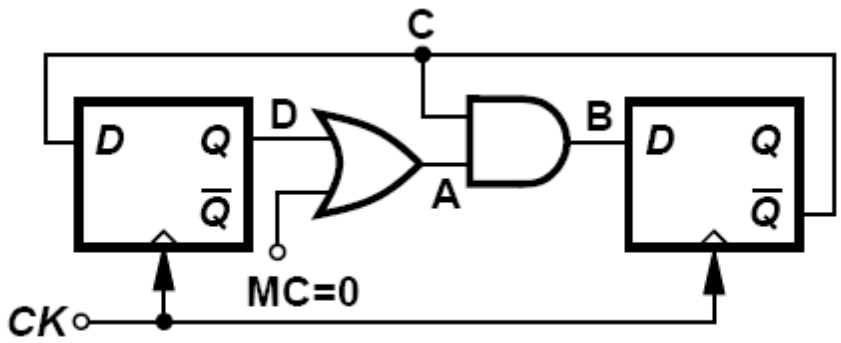
$$f_{out} = \frac{f_{in}}{NP+S}$$

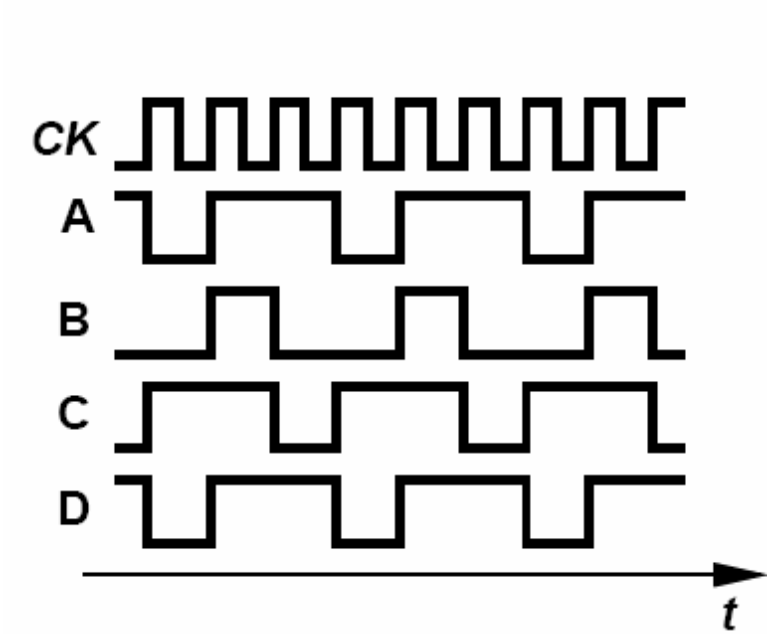
- Start from reset, prescaler divides by $N+1$ until swallow counter is full.
- After $(N+1)S$ pulses at the input, the modulus control changes to N.
- Continues to count until program counter is full.

$\Rightarrow$ Total pulses at the input = $(N+1)S+N(P-S) = NP+S$.

Prescaler (Dual-Modulus Dividers)

- ÷3/2 Divider

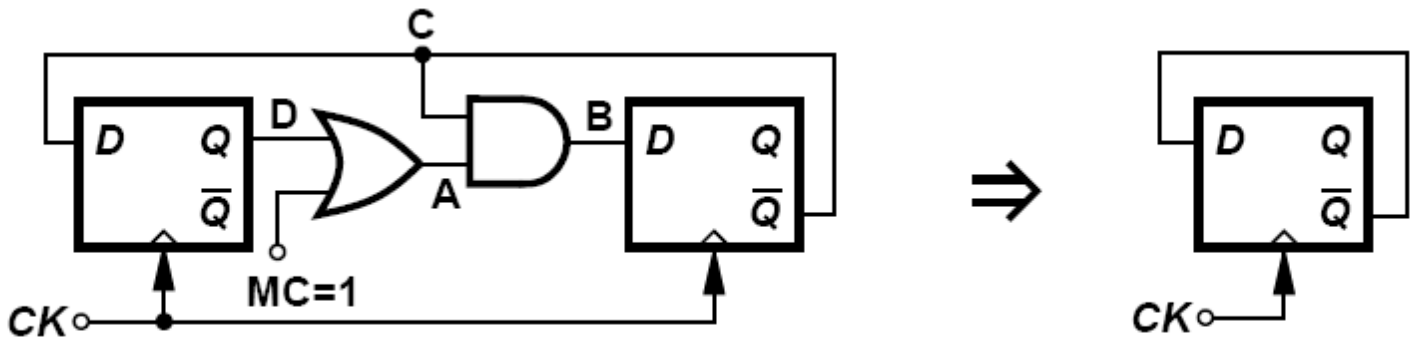




  - When MC=0 ⇒ OR Gate transparent ⇒ ÷3

Prescaler (Dual-Modulus Dividers)

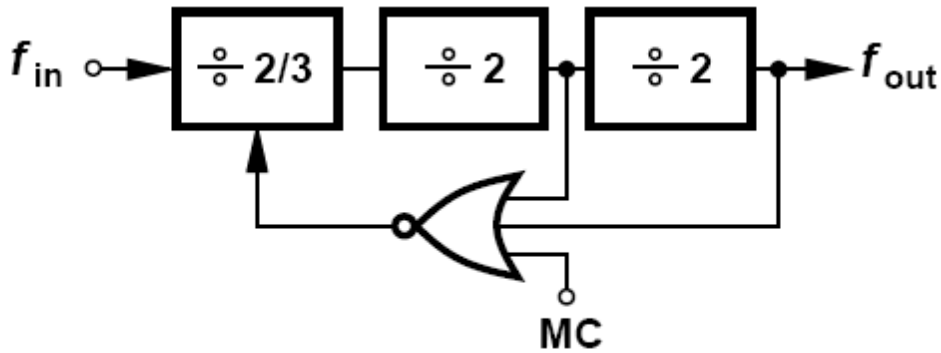
- ÷3/2 Divider



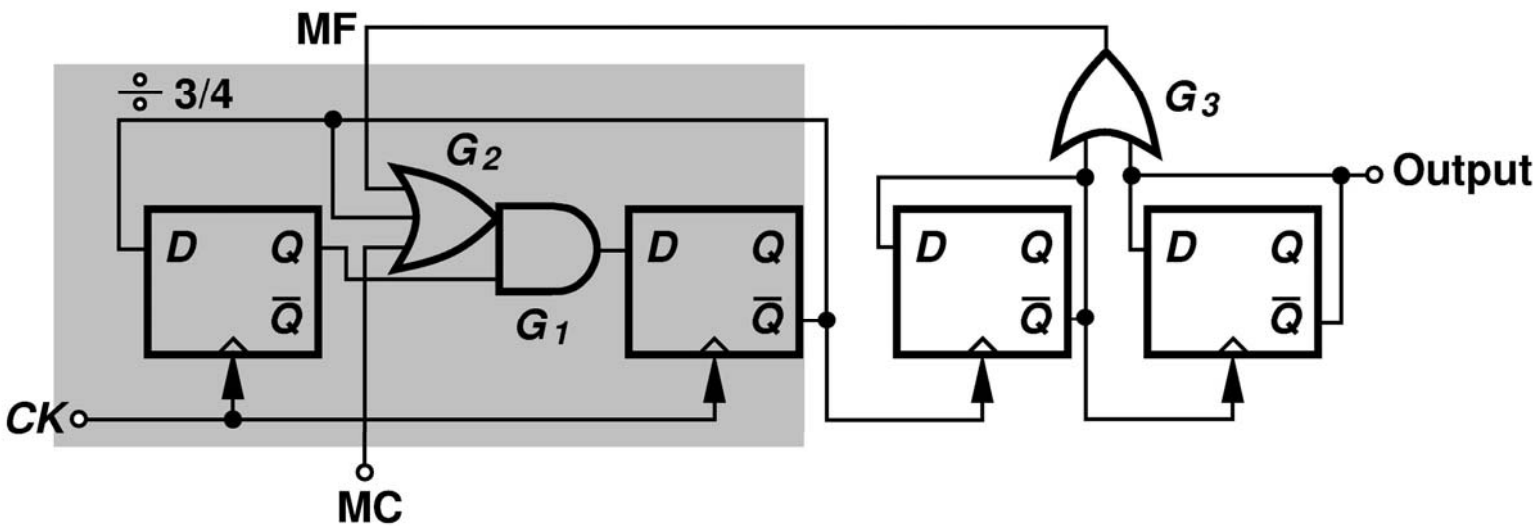
- When MC=1 ⇒ A=1, B=C ⇒ degenerates to ÷2 circuit

Higher Modulus Prescaler

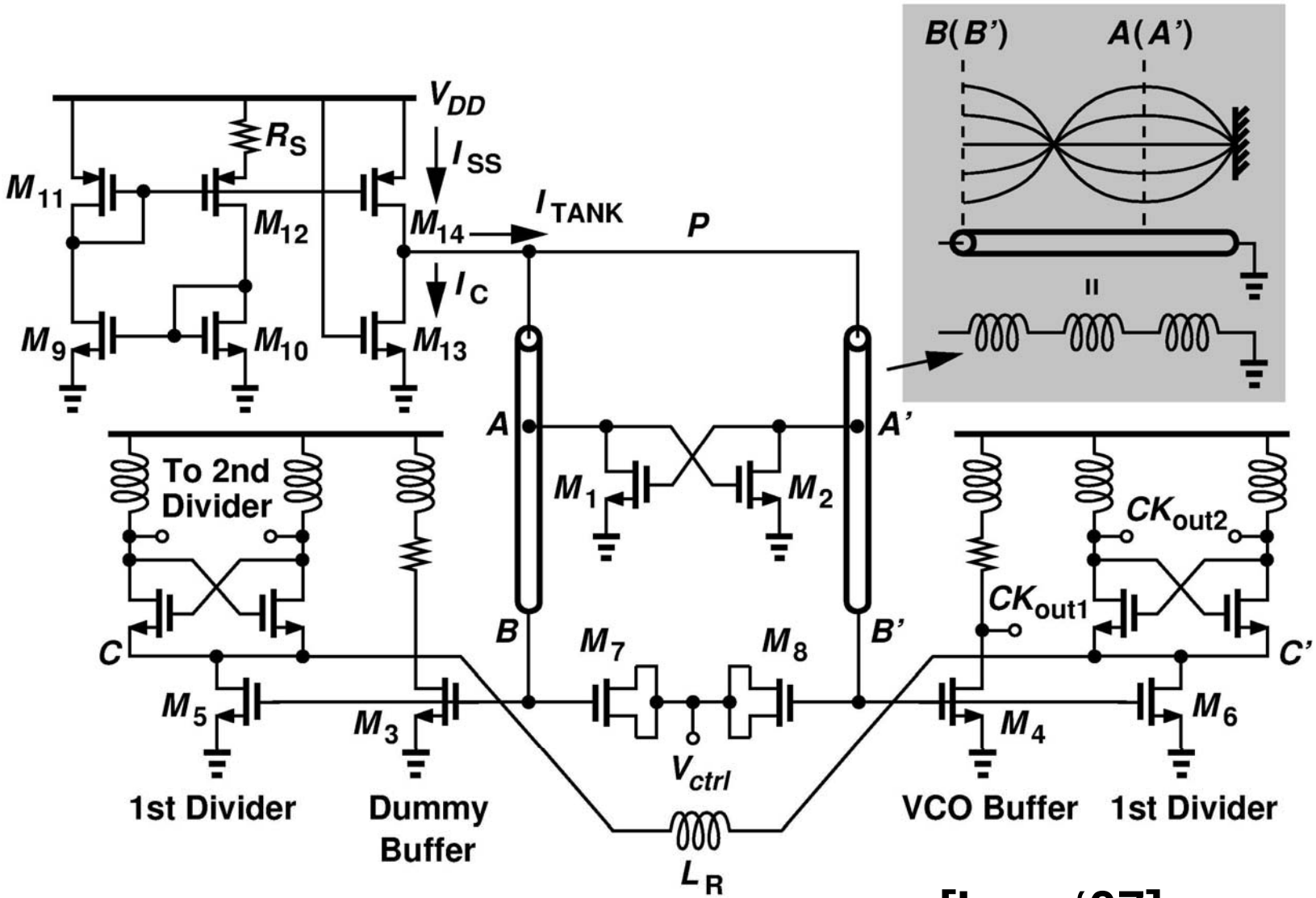
- ÷8/9 Divider



- ÷15/16 Divider



Case Study



[Lee, '07]