Part 01: Proposal and Overview

Dual Modulus Prescaler Using Current Mode Logic

Goals

- 2.5 GHz Operation
- 8/9 Dual Modulus
- 0.18uM BSIM 3 Model

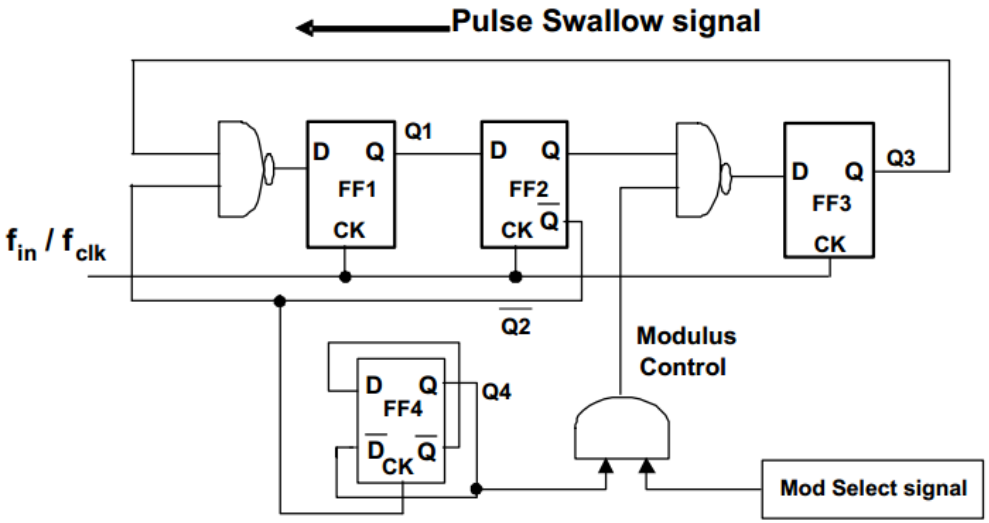


FIGURE 4.1: 8/9 Dual-Modulus Prescaler System.

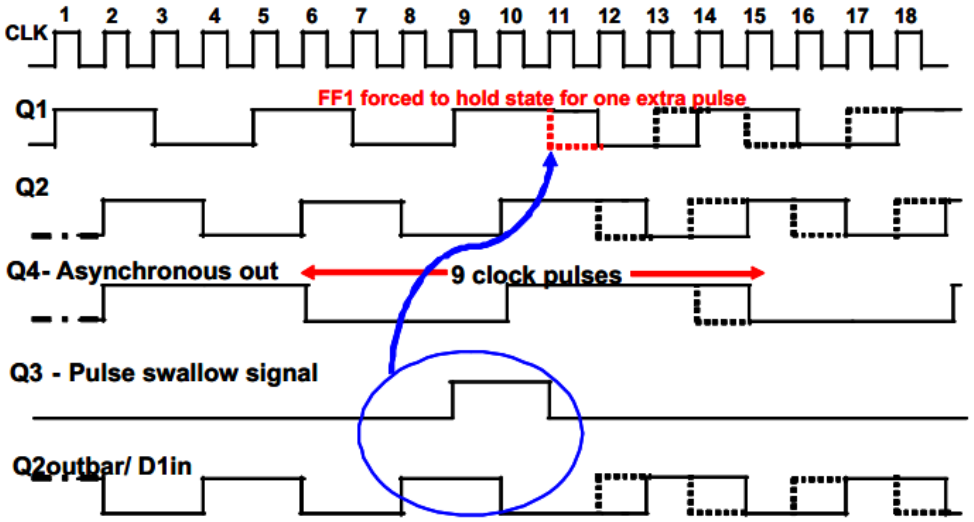


FIGURE 4.2: Timing diagram explanation of pulse-swallow operation.

D Flip Flop Schematic

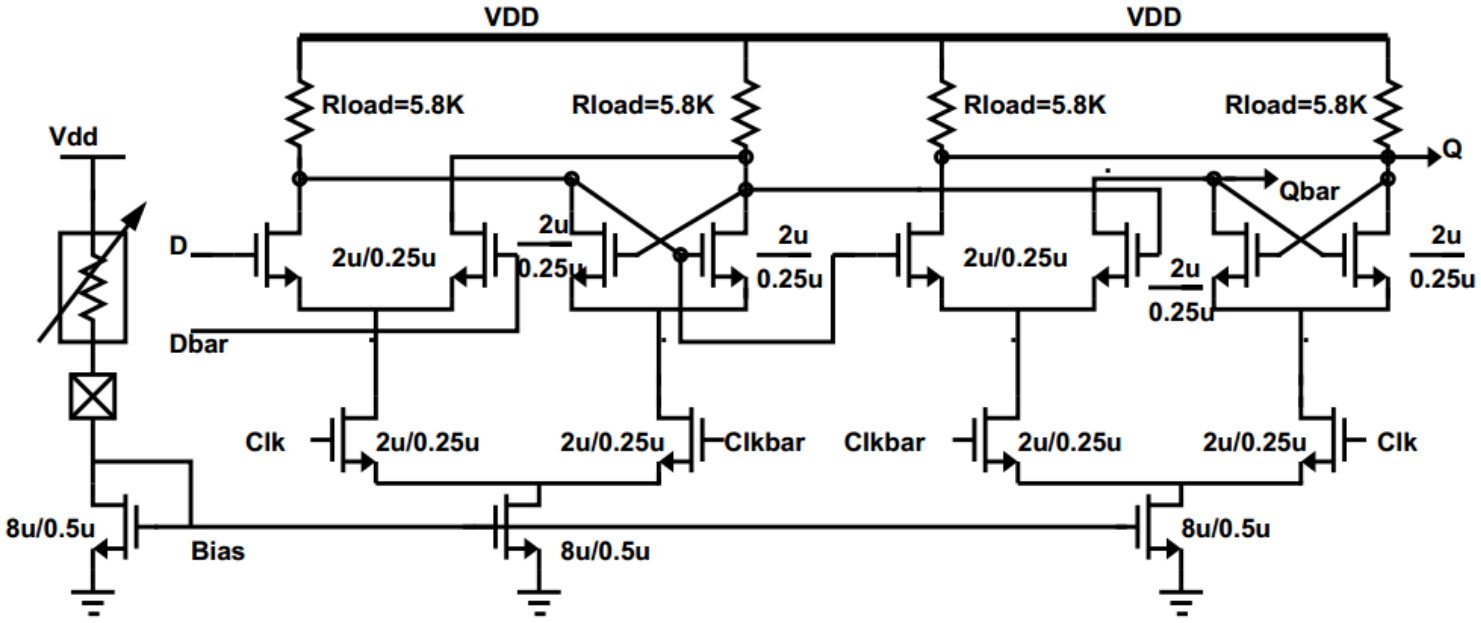


FIGURE 4.6: Optimized D flip-flop

Merged NOR for faster circuits

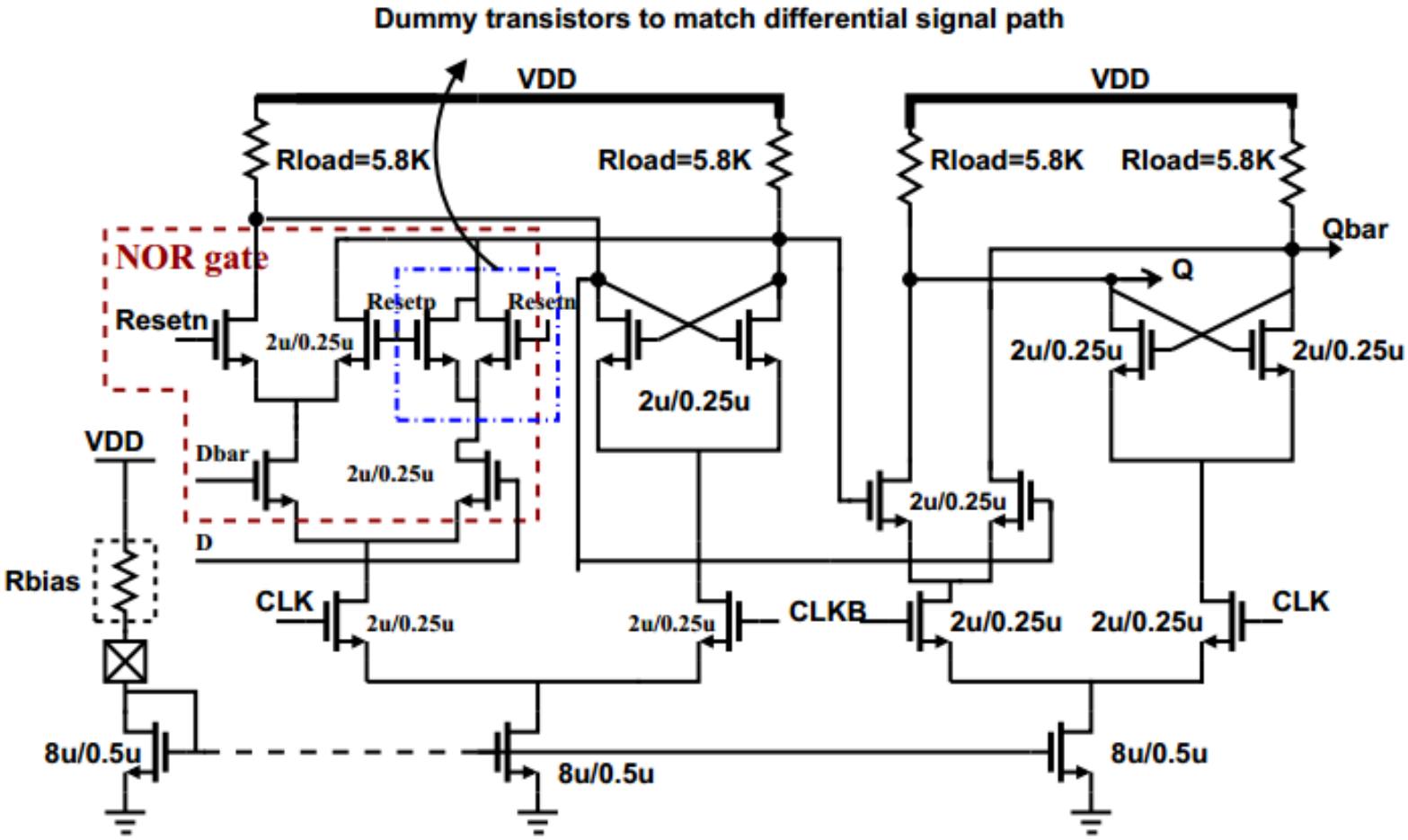


FIGURE 4.13: Flip-Flop3 with dummy devices to maintain signal symmetry.

Synthesizer Block Diagram

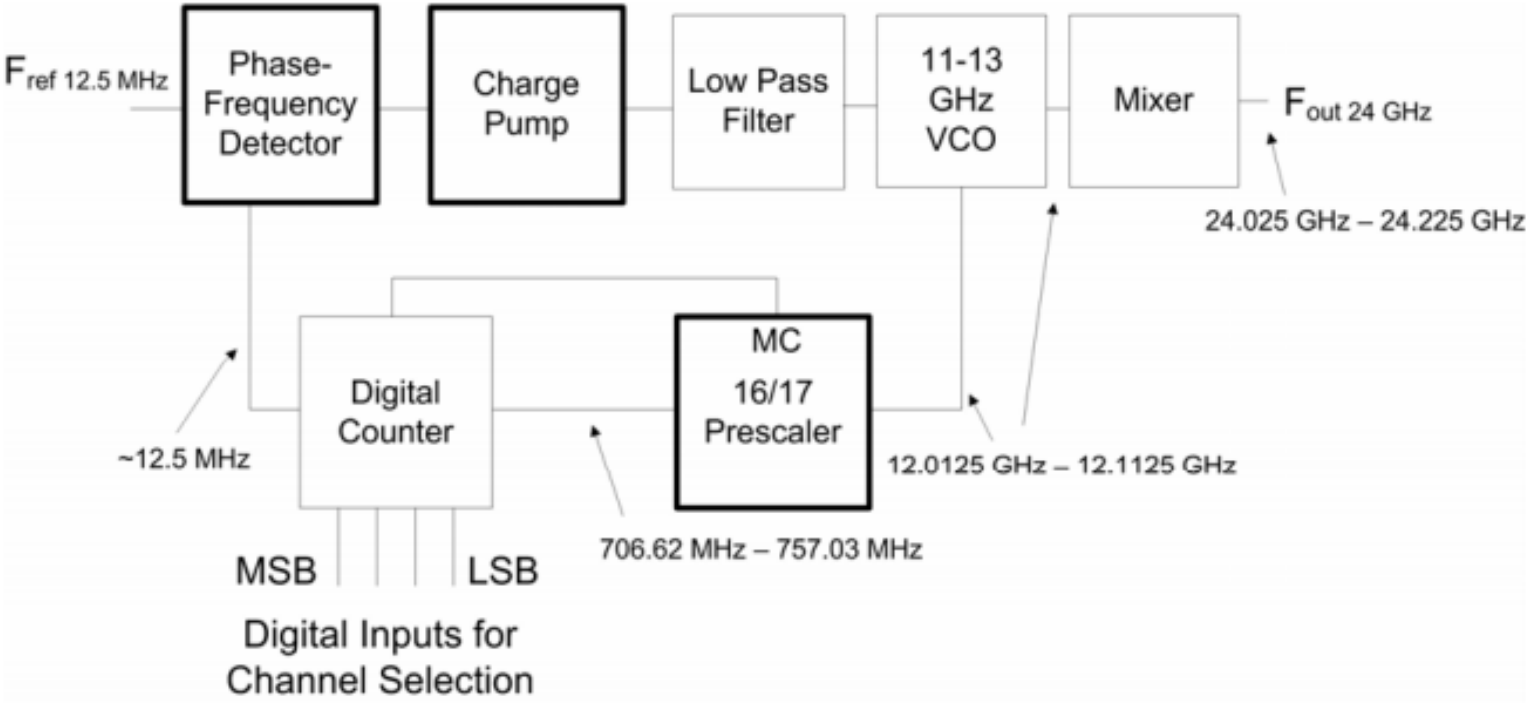
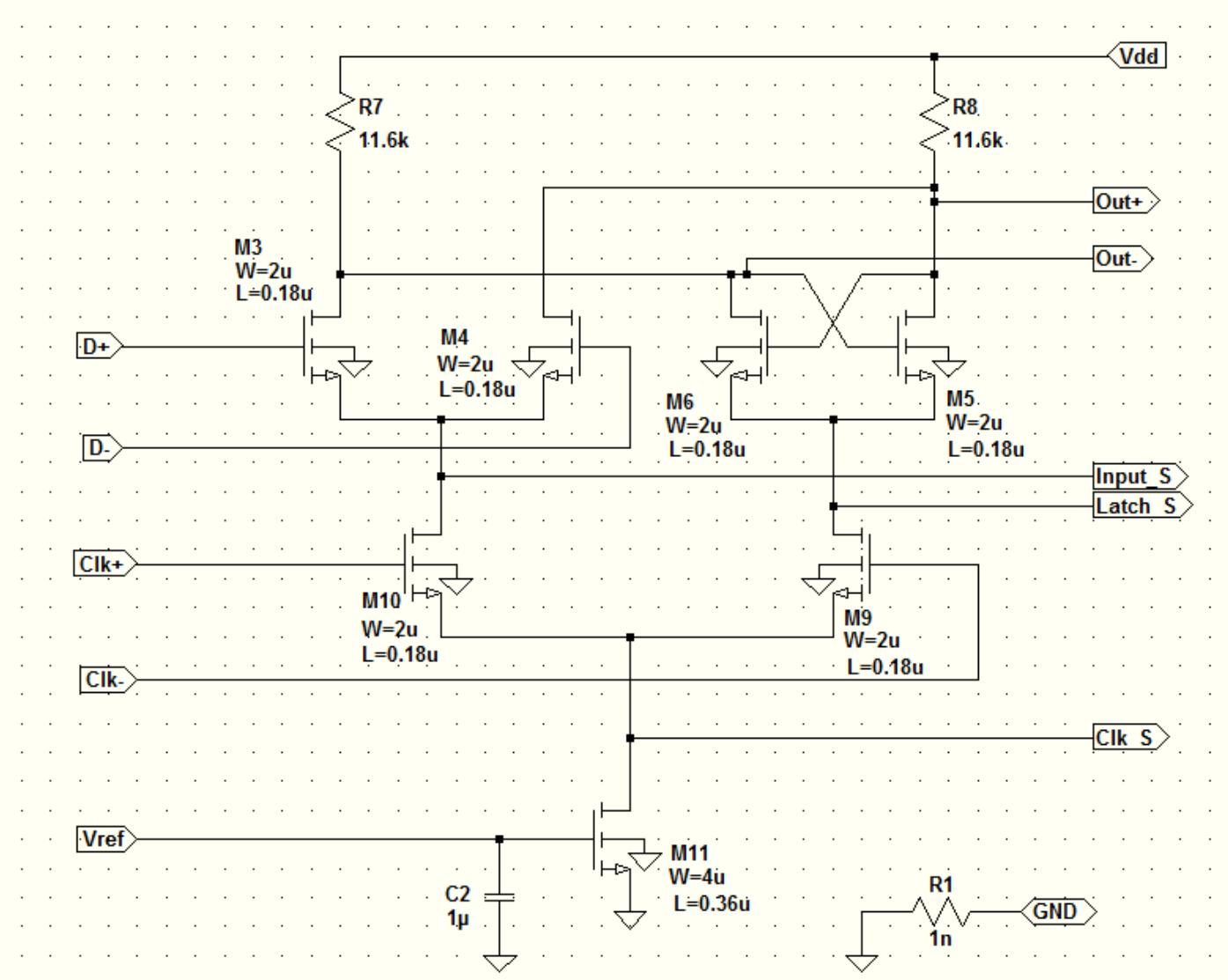


Figure 1: Block Diagram for 24 GHz Frequency Synthesizer

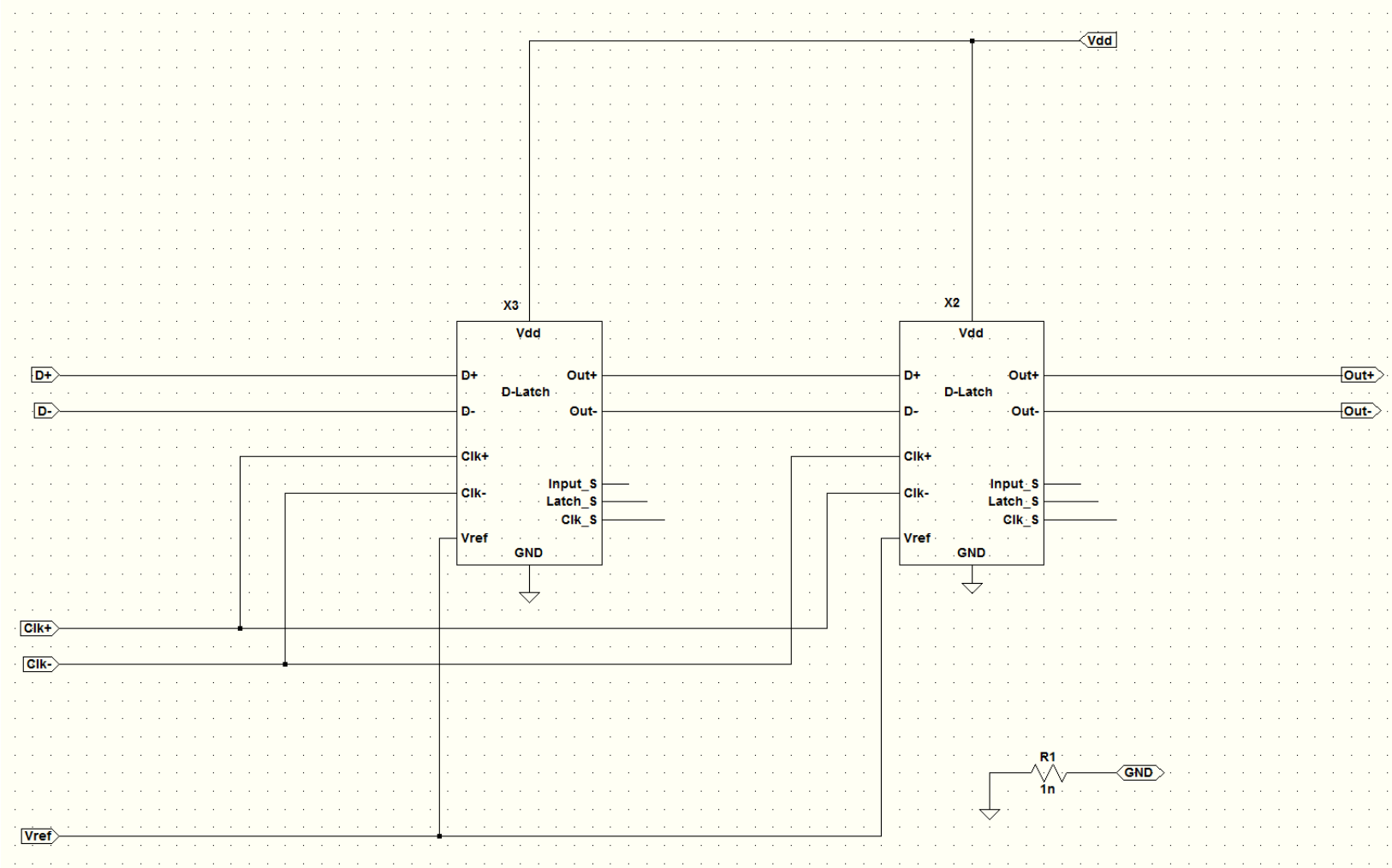
Part 02: Initial Efforts

- LTSPICE with MOSIS 180nM SPICE model

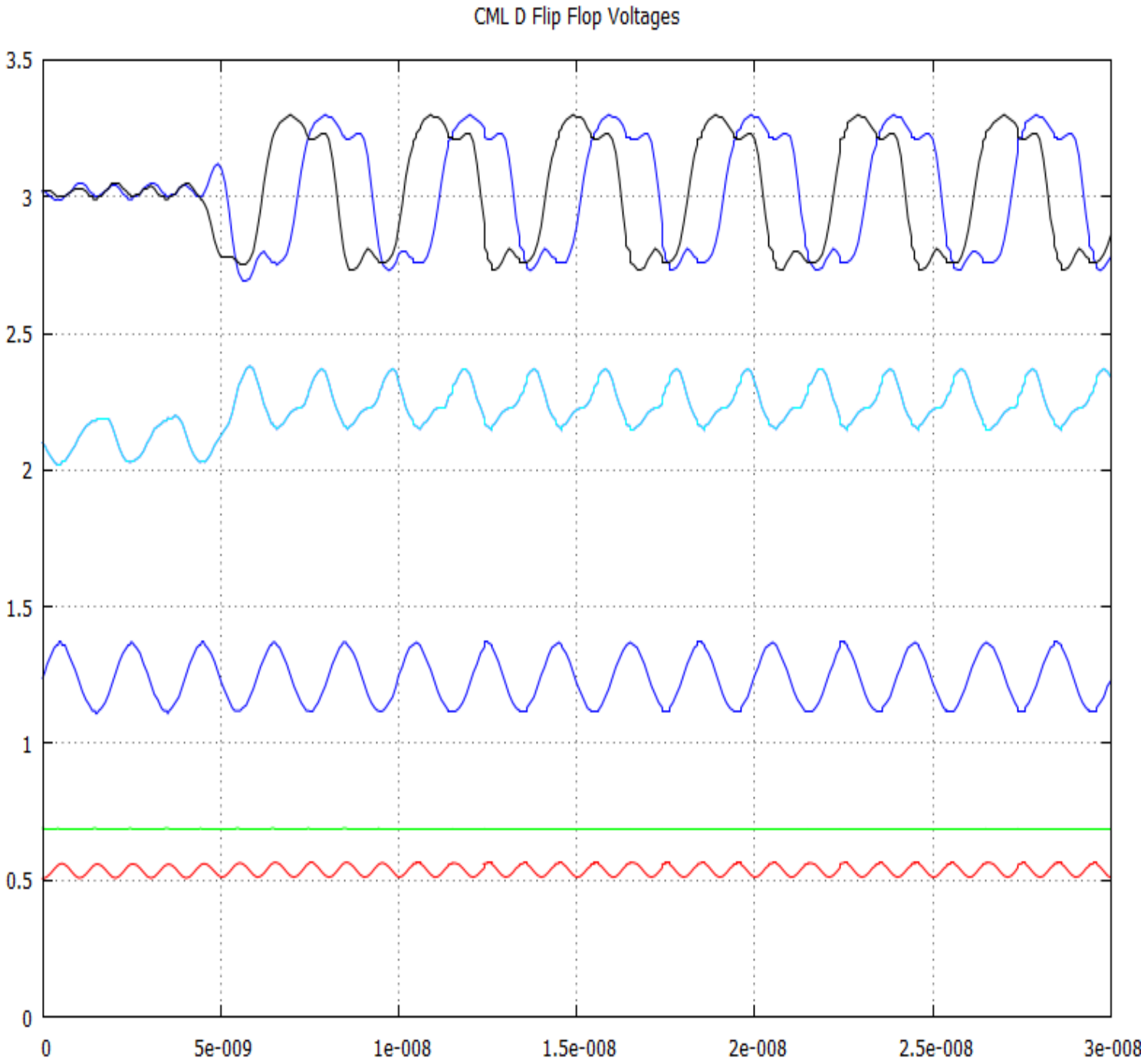
D Latch Schematic



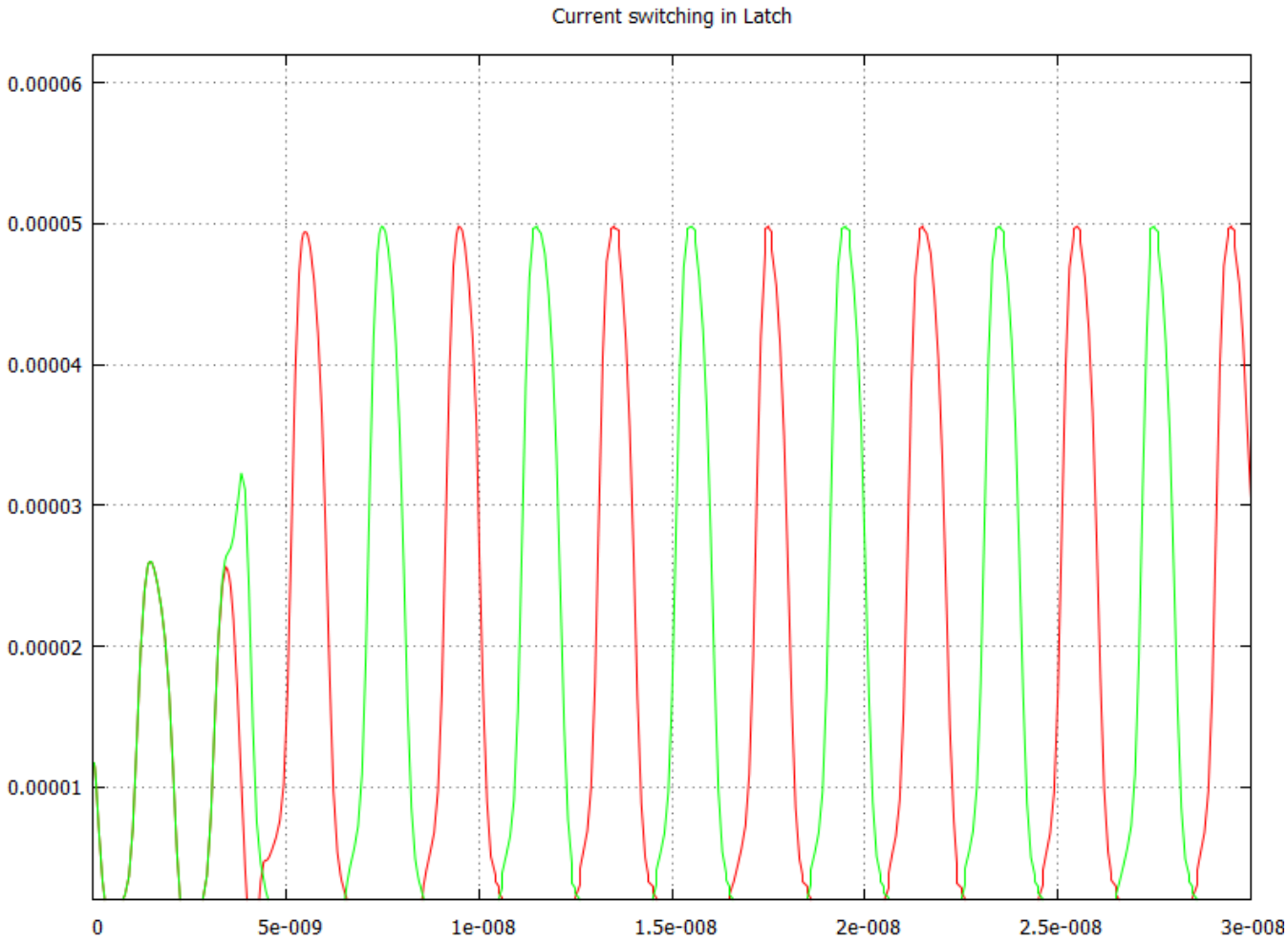
D Flip Flop Schematic



- Latch Out
- D FET Out
- D FET Source
- Input 500MHz
- Tail Gate V
- Tail Drain V



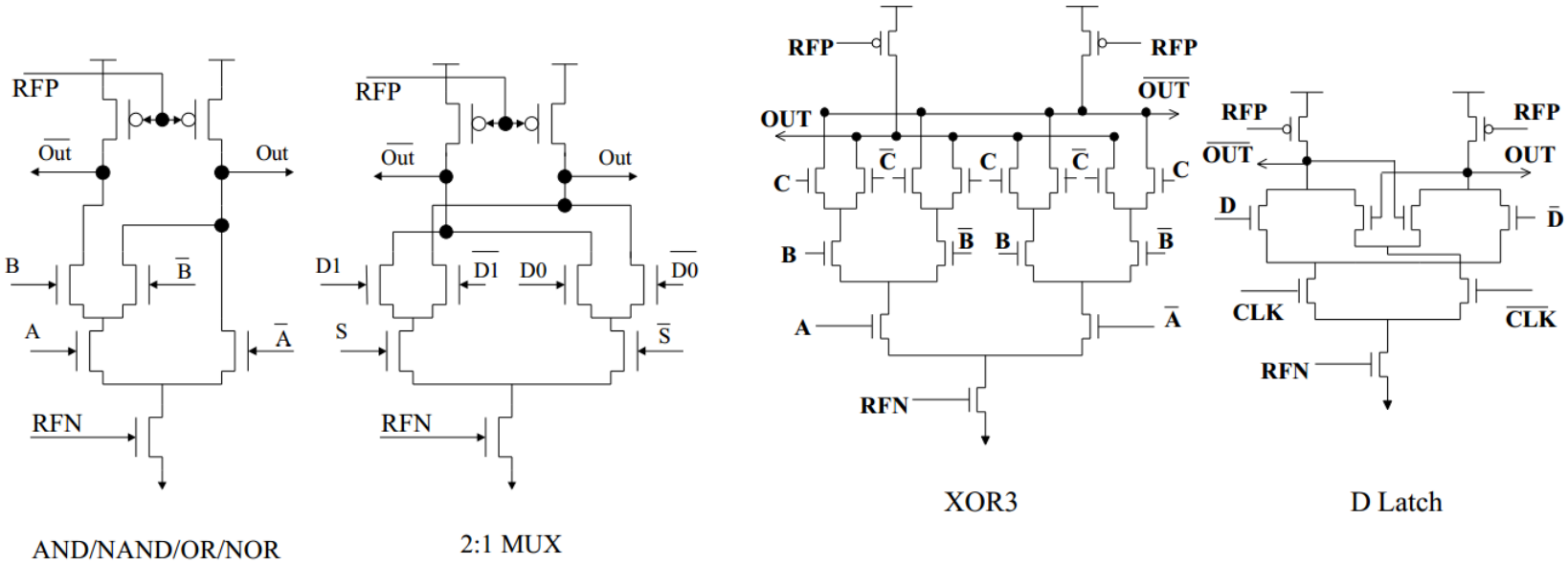
Latch Current Switching



Current from Clk- alternates flow through latch transistors

NOTE: 2 clock cycles required for valid data to show up on D flip flop output divider circuit

CML Gate Examples



AND/NAND/OR/NOR

2:1 MUX

XOR3

D Latch

Figure 2.3c : MCML Gate Examples

Logic Implementation Example

$$F = A[BC+B'D+CD] + A'[B'D+BC']$$

$$F = A[B(C+CD) + B'(D+CD)] + A'[B(C') + B'(D)]$$

$$F = A\{B(C) + B'(D)] + A[B(C') + B'(D)]$$

The BDD for this expression is shown in figure 2.3a and the implementation of the pull down network is shown in figure 2.3b.

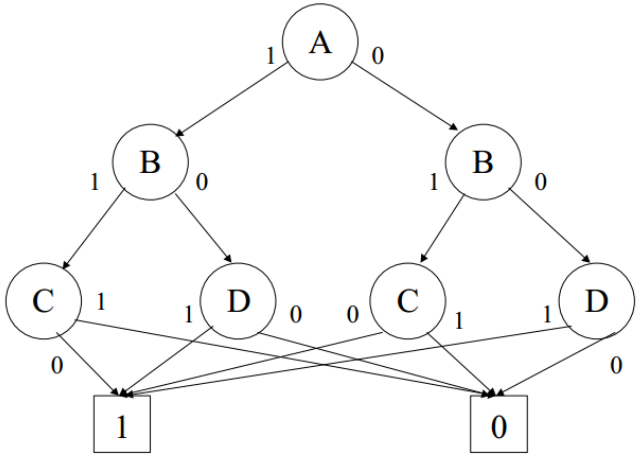


Figure 2.3a : Binary Decision Diagram for F

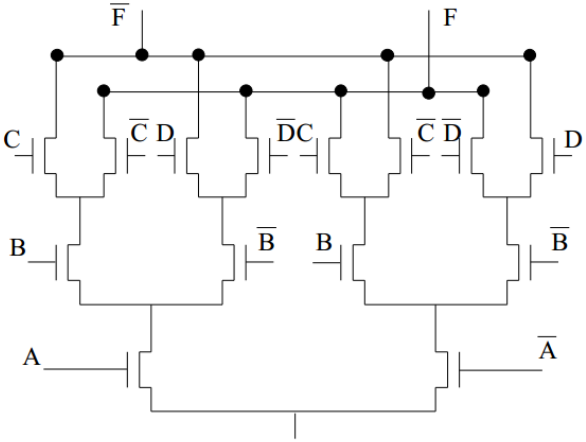
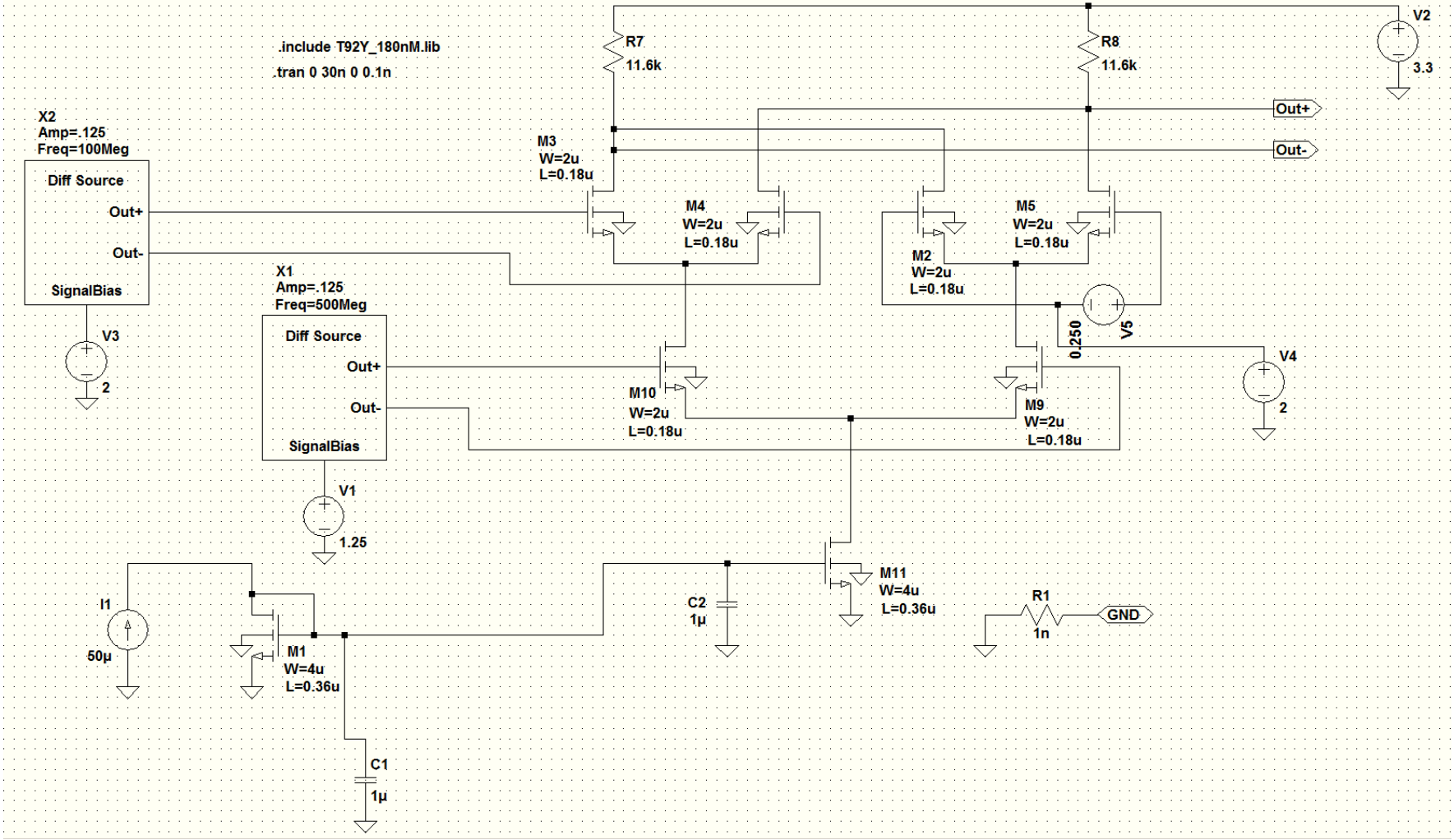


Figure 2.3b : MCML Pull Down Network for F

And Nand Or Nor Topology Design



Part03: Analysis of CML Bias / Design / Logic Levels

- Differential pair input range

If both M_1 and M_2 operate in weak inversion, the relationship between the differential output current and the differential input voltage is

$$\frac{I_{OD}}{I_T} = \frac{I_1 - I_2}{I_T} = \tanh\left(\frac{V_{ID}}{2n\phi_t}\right). \tag{7.5.5}$$

Formula (7.5.5) shows that the differential output current does not change significantly if the differential input voltage is greater than $4n\phi_t$, for any inversion level, as can be seen in Figure 7.17 for $I_T/I_S < 1$ and in Figure 7.18, where I_1, I_2, and the difference between them are plotted.

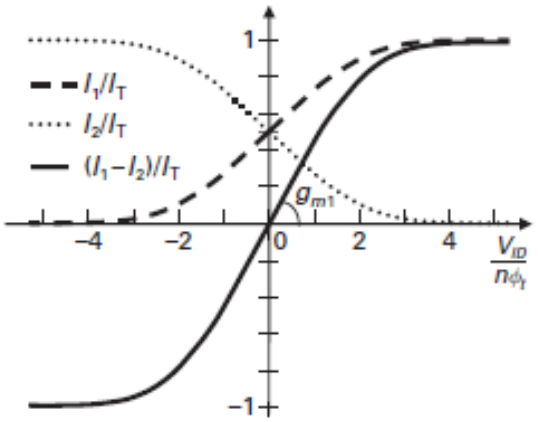


Fig. 7.18 The dc transfer characteristics of the differential pair in weak inversion.

Strong Inversion Diff Pair Input Range

On the other hand, the differential output current in strong inversion is

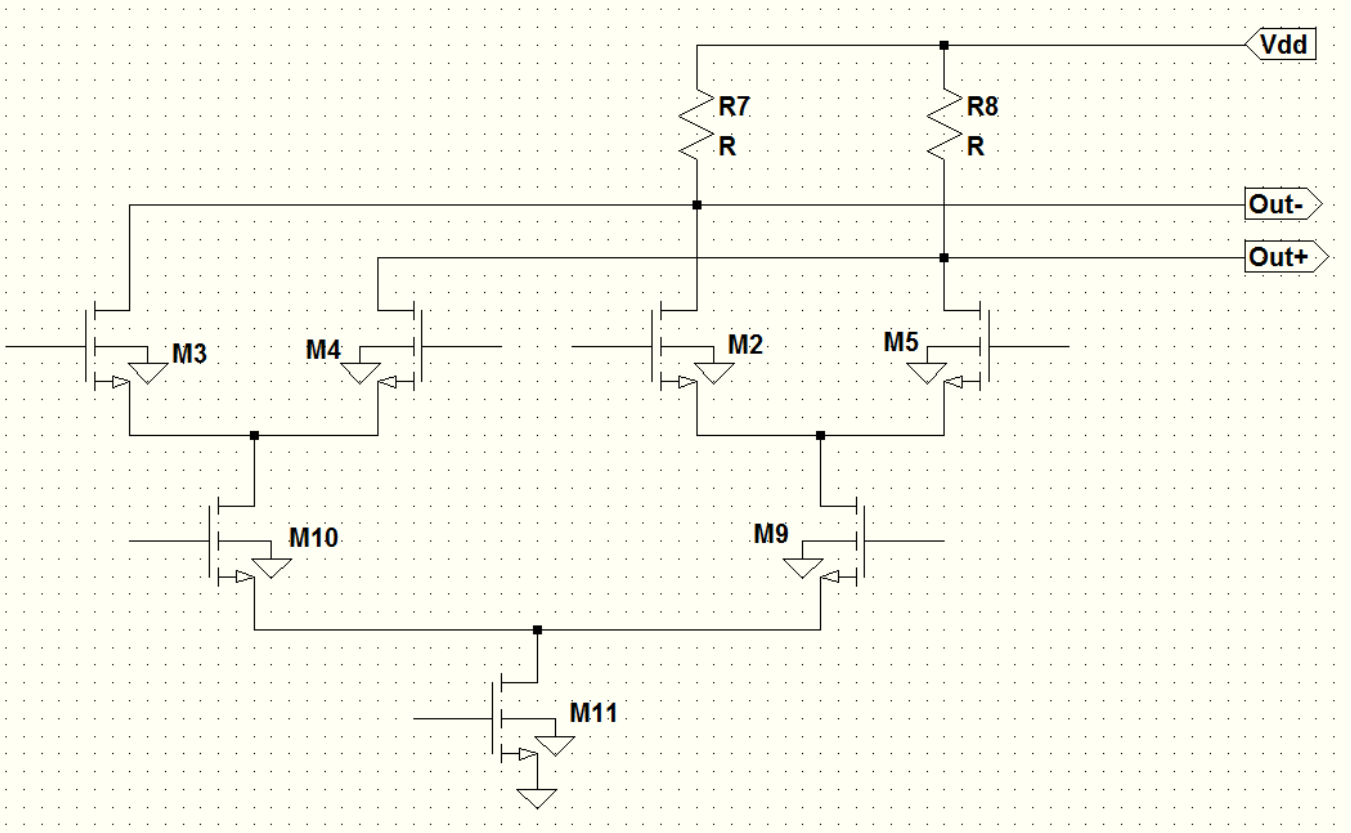
$$\frac{I_{OD}}{I_T} = \begin{cases} \dfrac{V_{ID}}{n\phi_t\sqrt{I_T/I_S}}\sqrt{2-\left(\dfrac{V_{ID}}{n\phi_t\sqrt{I_T/I_S}}\right)^2} & \text{for } \dfrac{|V_{ID}|}{n\phi_t\sqrt{I_T/I_S}} \le 1, \\ 1 \quad \text{for } \dfrac{V_{ID}}{n\phi_t\sqrt{I_T/I_S}} > 1, \\ -1 \quad \text{for } \dfrac{V_{ID}}{n\phi_t\sqrt{I_T/I_S}} < -1. \end{cases} \tag{7.5.6}$$

The output current saturates ($|I_{OD}| = I_T$) for $|V_{ID}| \ge n\phi_t\sqrt{I_T/I_S}$.

From Page 253 Galup/Schneider

$$n\phi_t\sqrt{\frac{I_{tail}}{I_{Specific}}}$$

High Diff Pair Common Mode of Output



$$V_{CM} = V_{DD} - \frac{I_{Tail} R}{2}$$

If $V_{CM} = \frac{V_{DD}}{2}$ then

$$I_{Tail} R = V_{DD}$$

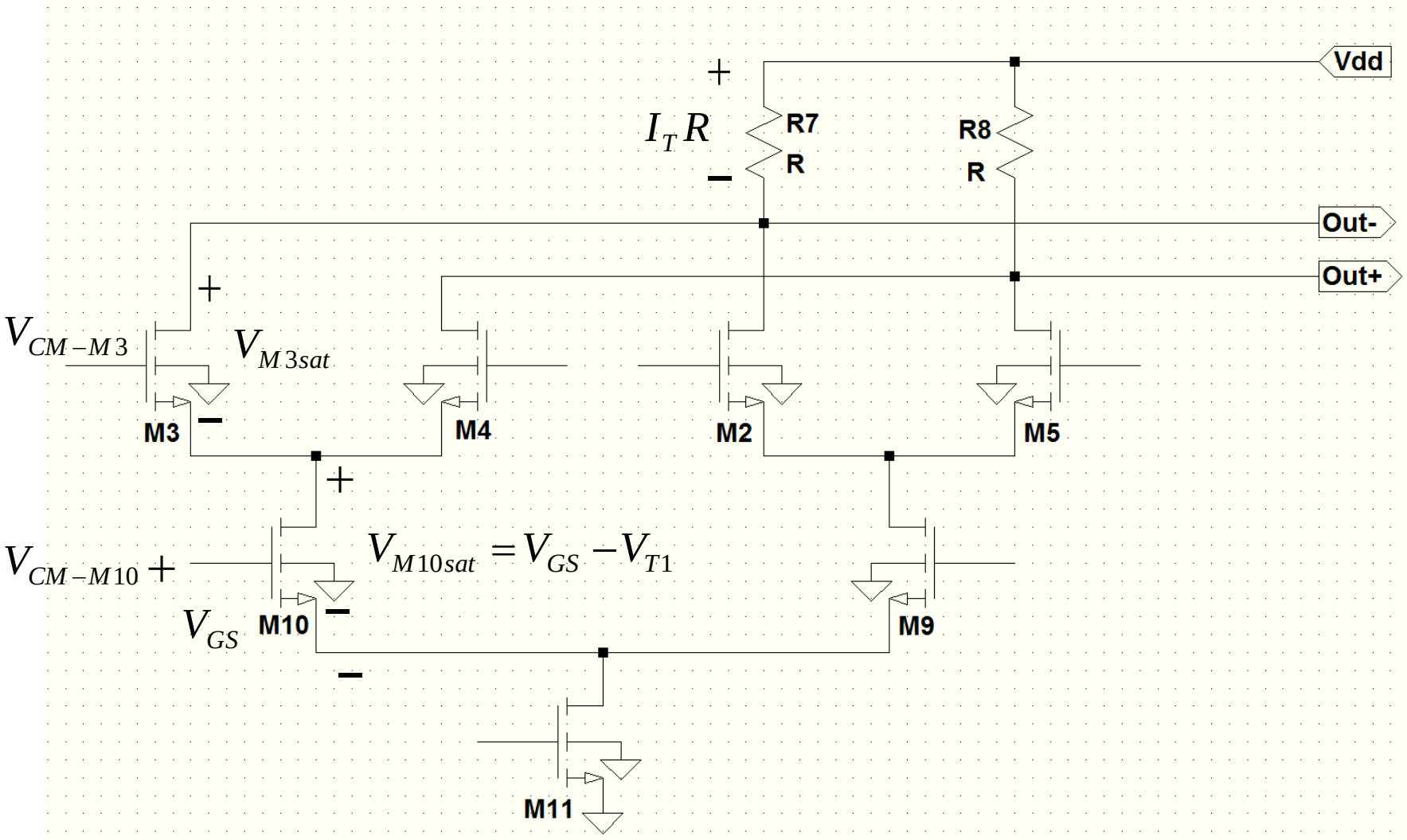
That means :

$$V_{Hi} = V_{DD}$$

$$V_{Lo} = 0$$

Common Mode Limits

- Assume transistors to be in saturation under all conditions
- Lower differential pair – Upper limit on common mode



Common Mode Limits

Lower differential pair – Upper limit on common mode

$$V_{S3} = V_{CMm3} - V_{GS3}$$

$$V_{M3sat} = V_{GS3} - V_{T3}$$

$$V_{GS3} = V_{M3sat} + V_{T3}$$

$$V_{S3} = V_{CMm3} - (V_{M3sat} + V_{T3})$$

Thus the maximum value of M10 drain is

$$V_{S3} = V_{CMm3} - V_{M3sat} - V_{T3}$$

Which means

$$V_{CMm10} \le V_{S3} + V_{T10} = V_{CMm3} - V_{M3sat} - V_{T3} + V_{T10}$$

Assuming :

$$V_{T3} = \sim V_{T1}$$

Then :

$$V_{CMm10} \le V_{CMm3} - V_{M3sat}$$

Common Mode Limits: Bottom Pair

Lower differential pair – lower limit on common mode

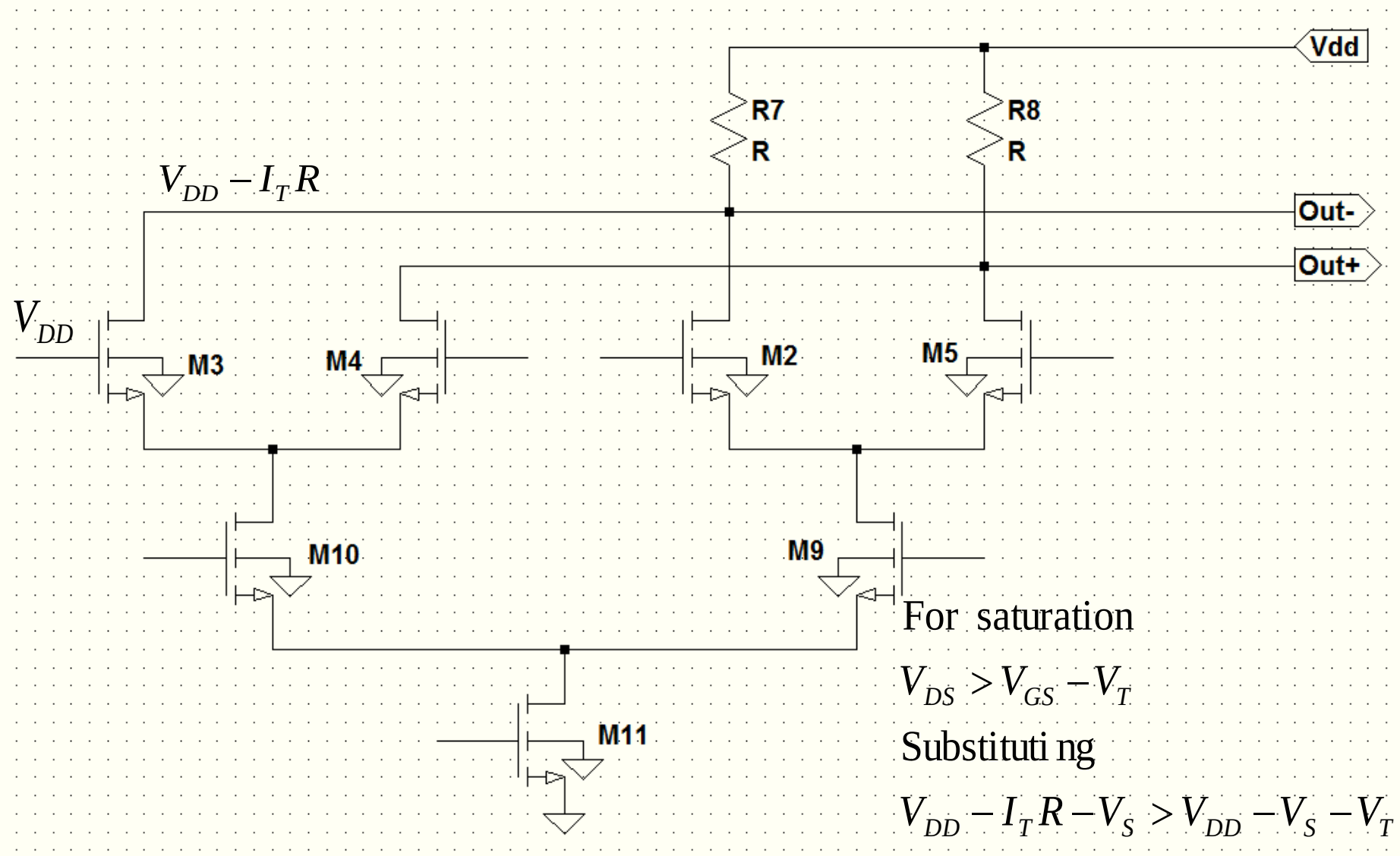
$$V_{CM} > V_{DSsatM11} + V_{DSsatM10} + V_{T10}$$

Putting it all together we can see the common mode of the lower pair can not be the same as the upper pair

$$V_{DSsatM11} + V_{DSsatM10} + V_{T10} \leq V_{CMm10} \leq V_{CMm3} - V_{M3sat}$$

Thus when driving the lower differential pair a level shifter is required.

Output Swing Limit



For saturation

$V_{DS} > V_{GS} - V_T$

Substituting

$V_{DD} - I_T R - V_S > V_{DD} - V_S - V_T$

thus :

$I_T R < V_T$

In order to maintain saturation: $I_T R < V_T$

See: Ref #1.P35, #3

Part 3A: Hand Design: Things we need

- Signal FETs L – Minimum length for maximum speed
- Signal FETs W – Simple low frequency analysis using interface criteria
- Current Source FET – L, W
- Tail Current – Assume a nominal value and optimize performance
- Swing
- Load Resistance

Hand Design Swing, Signal FET W & L

- As previously cover swing should be on the order of Vt
- Choose 0.6V
- Calculate required width of signal FET using inversion level required to have full current drive + gate over drive
- Use gate over drive of 0.300V to insure adequate input drive.
- Thus Vid=~0.300V

$$V_{ID} = n\phi_t \sqrt{\frac{I_{tail}}{I_{Specific}}}$$

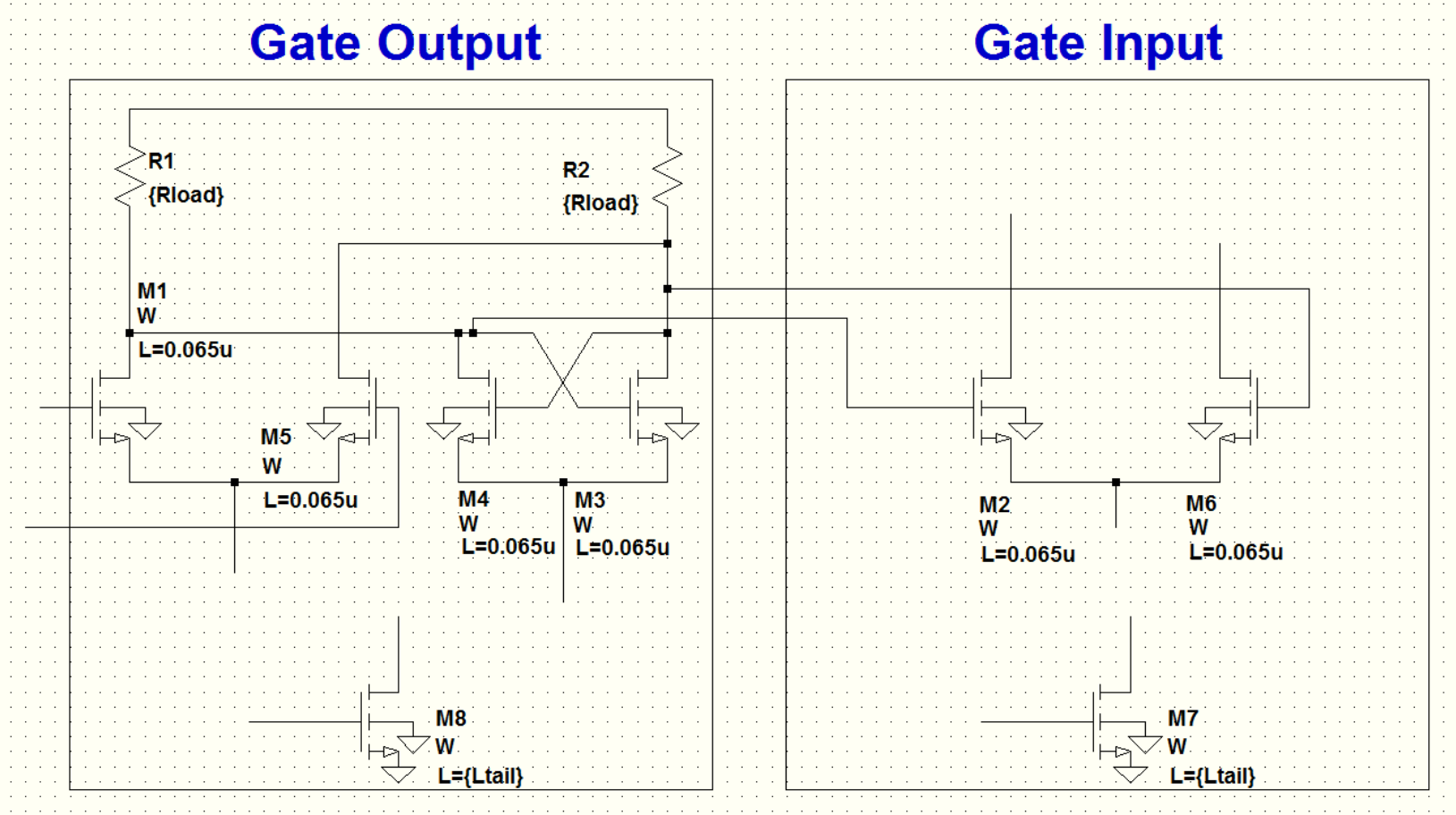
$$0.300 = 1.6 * 0.025 \sqrt{\frac{100uAmp}{I_{Specific}}}$$

$$I_{Specific} = 3.7uAmp$$

Since Ispecific of unit width = 1uM is ~2uAmp use W=2uM

(See Appendix 1 for extraction of MOSFET parameters Vt, Ispecific and n the slope factor

Hand Design: Output == Input



Resistive Loads $V_{Swing} = 0.6$

$I_{Tail} = 100uAmp$

$R_{Load} = 6kOhm$

Hand Design: Current Source Tail MOSFET

- Assume tail Vds = 0.350V well into saturation region
- Assume Ltail = 10 x Lmin for the tail impedance to be large compared to signal FET

$$L_{Tail} = 0.65uM$$

$$V_{DS} = 0.350Volts$$

To be safe assume onset of saturation to be at $V_{Sat} = 0.250Volts$

$$V_{Sat} = \phi_T (3 + \sqrt{1 + i_f})$$

$$i_f = \left(\frac{V_{Sat}}{\phi_T} - 3 \right)^2 - 1$$

$$i_f = \left(\frac{0.250}{0.025} - 3 \right)^2 - 1 = 48$$

$$i_f = 48 = \frac{I_{Tail}}{I_{Specific-Tail}} = \frac{100uA}{I_{Specific-Tail}}$$

$$I_{Specific-Tail} = 2uA = \frac{W_{Tail}}{L_{Tail}} I_{Square} \quad \text{From previous calculations : } I_{Square} = 0.13uA$$

$$2uA = \frac{W_{Tail}}{0.65uM} 0.13uA$$

$$W_{Tail} = 10uM$$

Hand Design MOSFET Summary

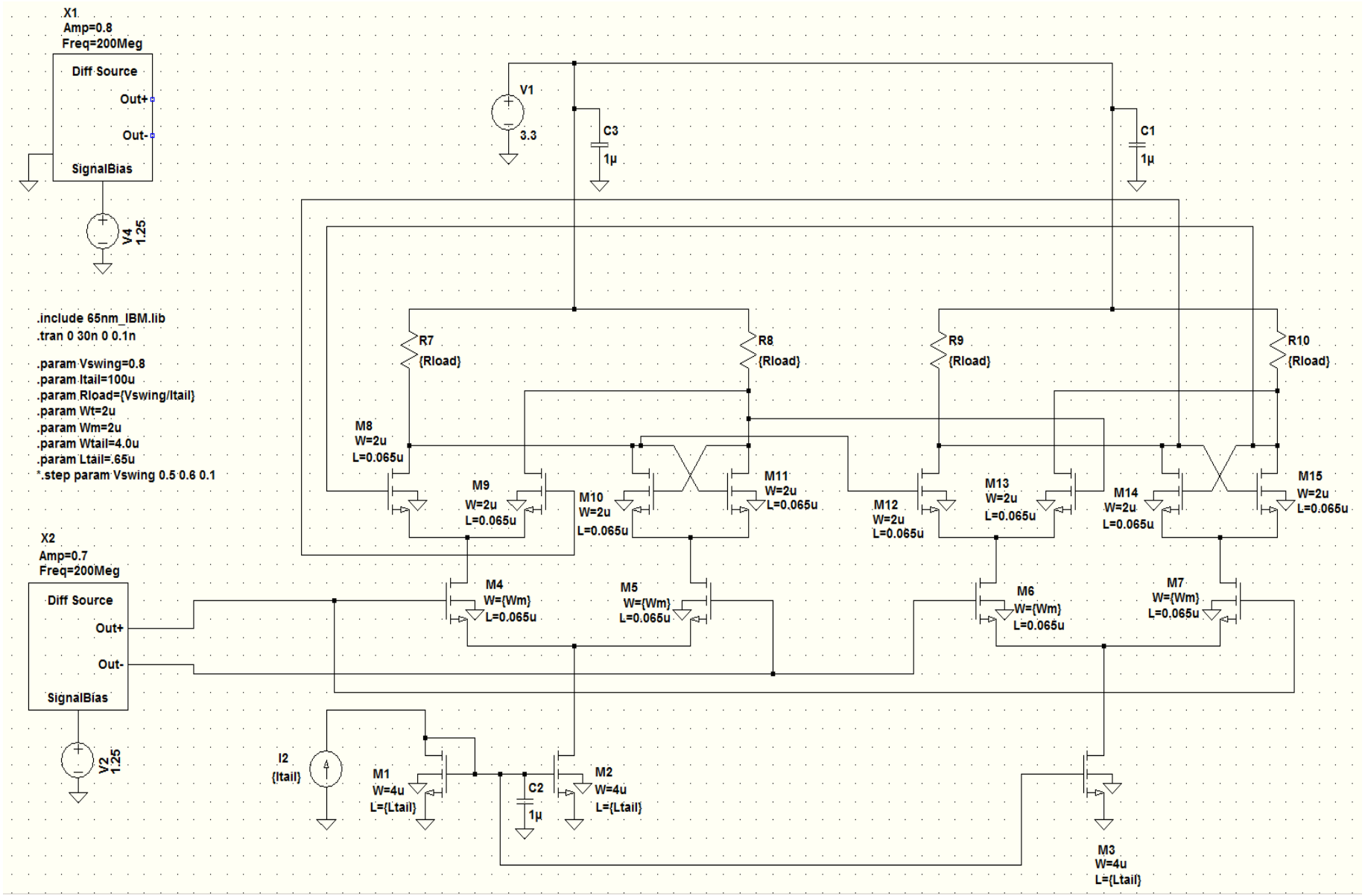
- Signal FET Width = 2uM
- Signal FET Length=0.065uM (Minimum)
- Tail FET Width = 10uM
- Tail FET Length=0.66uM

Increasing Tail FET width & Length will probably more than this will probably run against increasing capacitance and not provide more benefit.

Part 04: Simulation: D Flip Flop in IBM 65nm

- MOSIS: IBM-Fishkill 65nm SPICE FILE

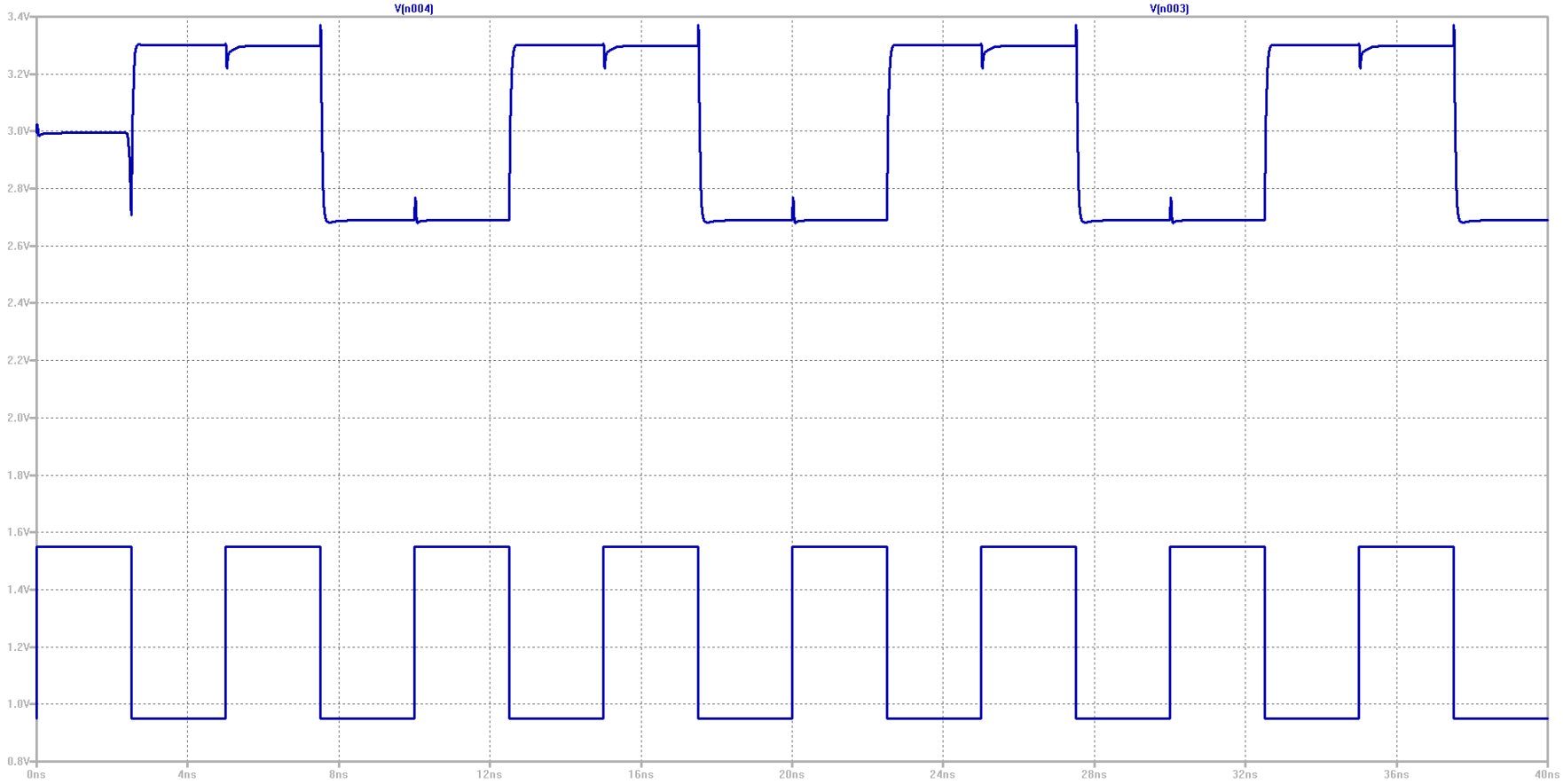
D Flip Flop Optimization



Optimization Parameters

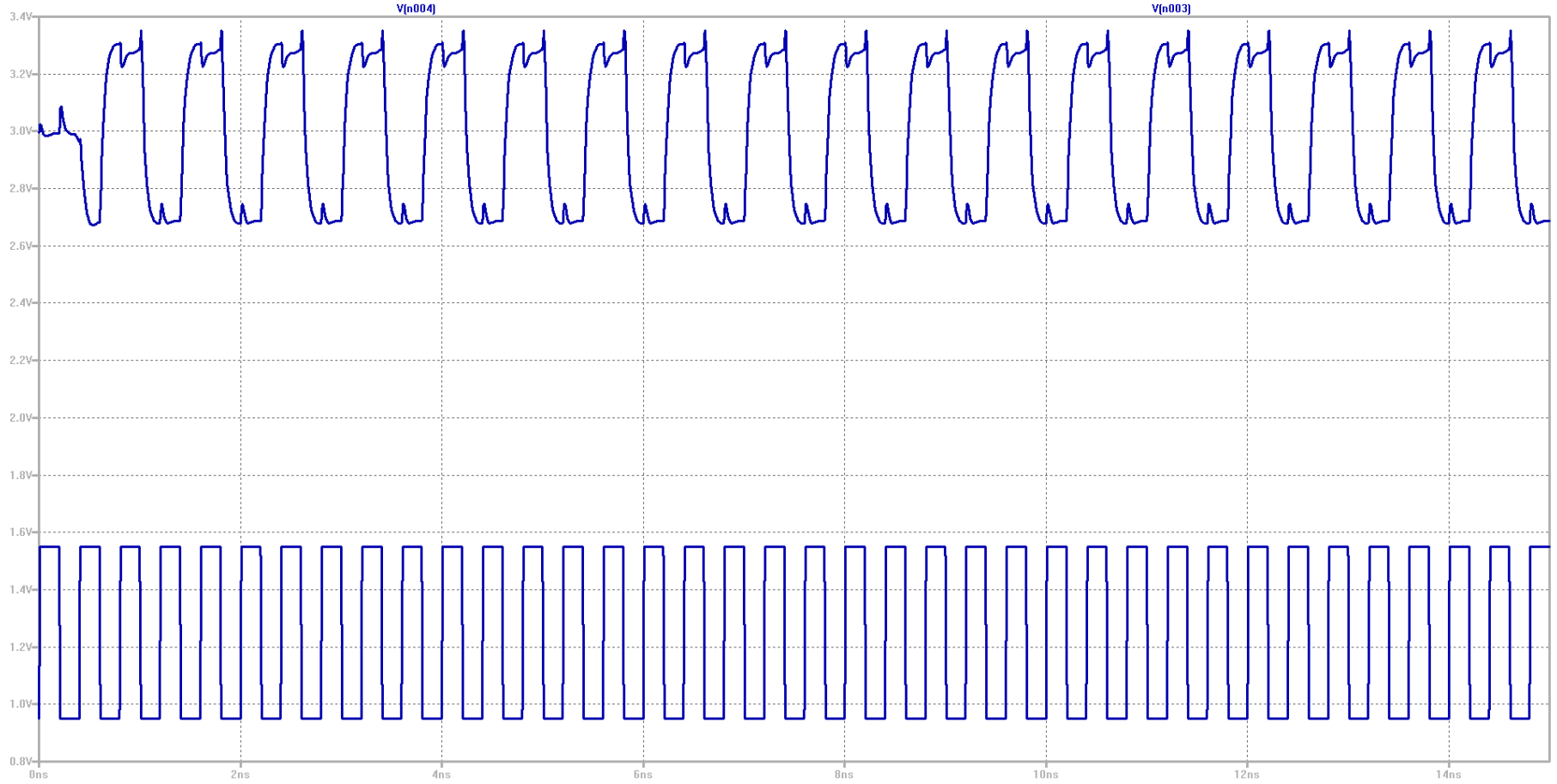
```
.include 65nm_IBM.lib
.tran 0 40n 0 0.1n

.param Vswing=0.6
.param Itail=100u
.param Rload={Vswing/Itail}
.param Wt=2u
.param Wm=2u
.param Wtail=10.0u
.param Ltail=.65u
*.step param Vswing 0.5 0.6 0.1
```

Slow 200MHz Waveforms to see the transients



- Minimum time to start divider is 1 rising + 1 falling edge
- The glitches are at clock cross over where there is a tail current spike
- Vswing=0.6V
- Fin=200 MHz

Operation At 2.5 GHz

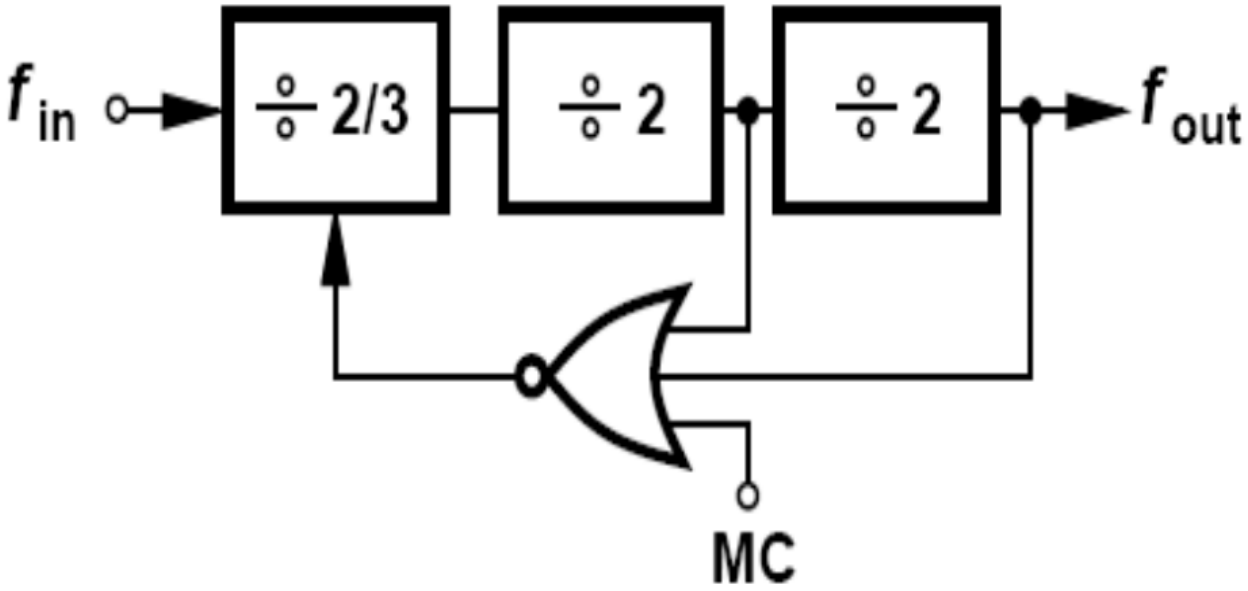


- Vswing=0.8V
- Fin=2.5GHz
- Divider start up takes more time clock cycles than 200MHz.
- Startup does not appear to be affected by swing once above a certain level

D Flip Flop Optimization

- Power is independent of frequency
- Power is independent of swing
- Power consumption = Vdd * Itail * NumTails
- Output waveform had better rise time for lower swing
  - However did not work when used with higher assembly
- Changes in signal MOSFET widths resulted in small changes in rise time
  - Going to Wt = Wm = 1u might be slightly better.
  - Much narrower or much wider resulted in worse rise times
- Works over -40 to +80 C

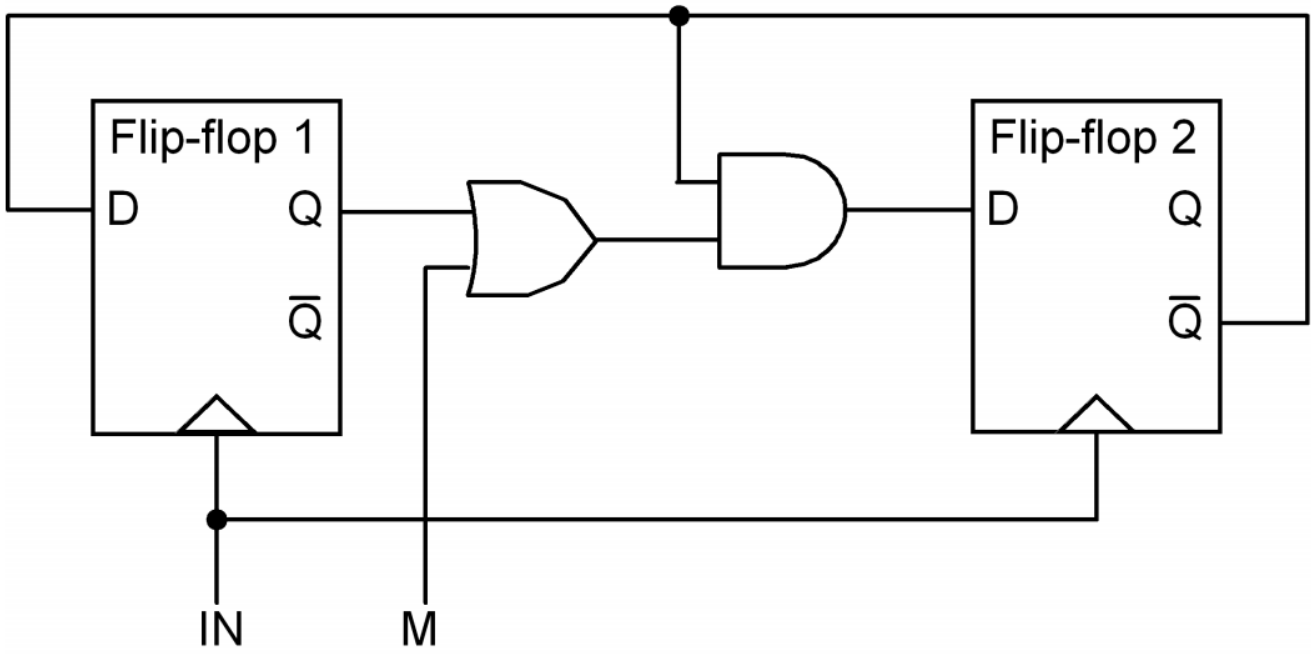
Part 5: Block Build Up



Modulus = 8/9 Prescaler (See Ref 5)

- 2/3 Prescaler
- D Flip Flop in /2 configuration
- 3 input OR gate

Sub-block: Modulus 2/3 Prescaler

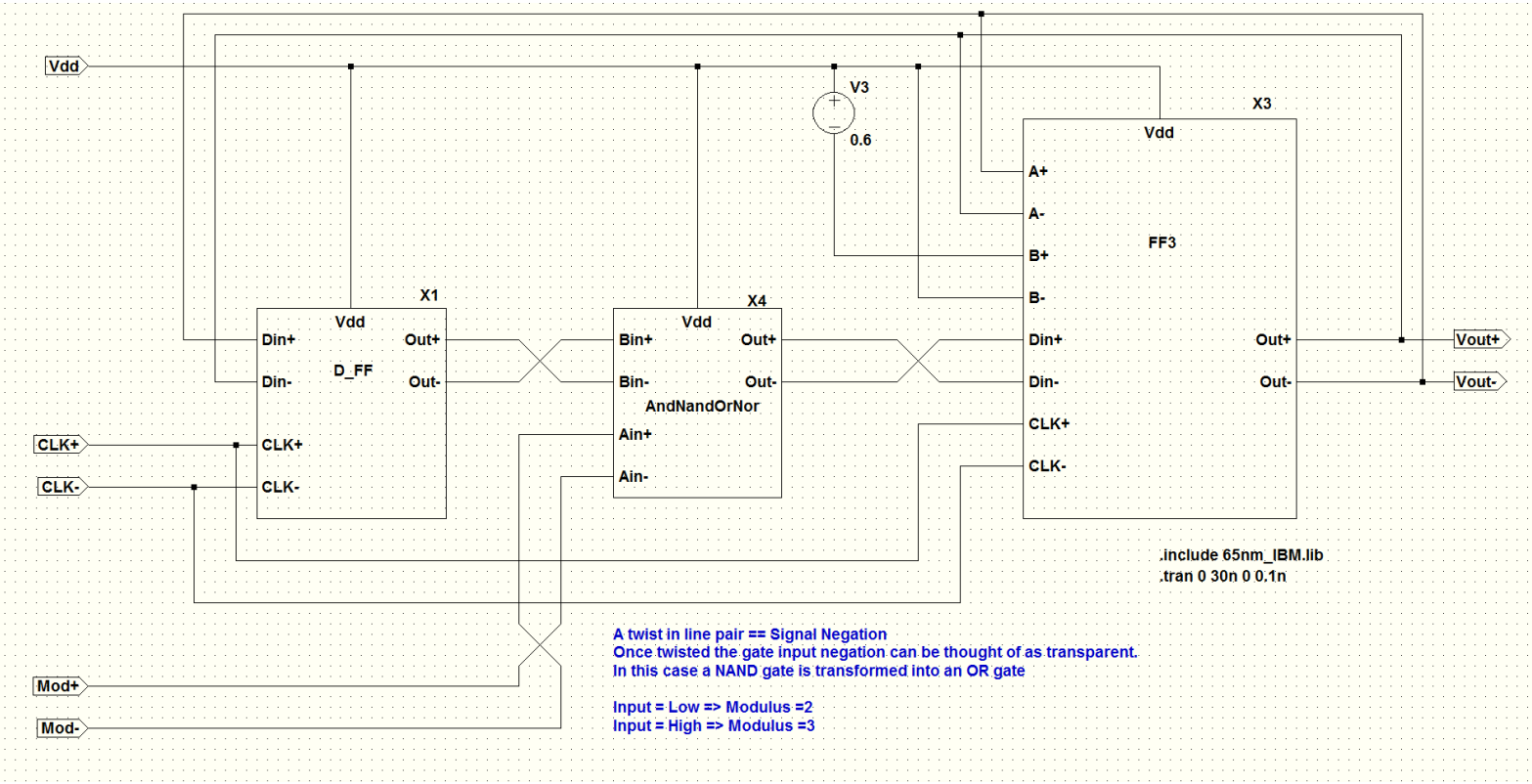


See Ref 6

Figure 2.5: $\div 2/3$ circuit

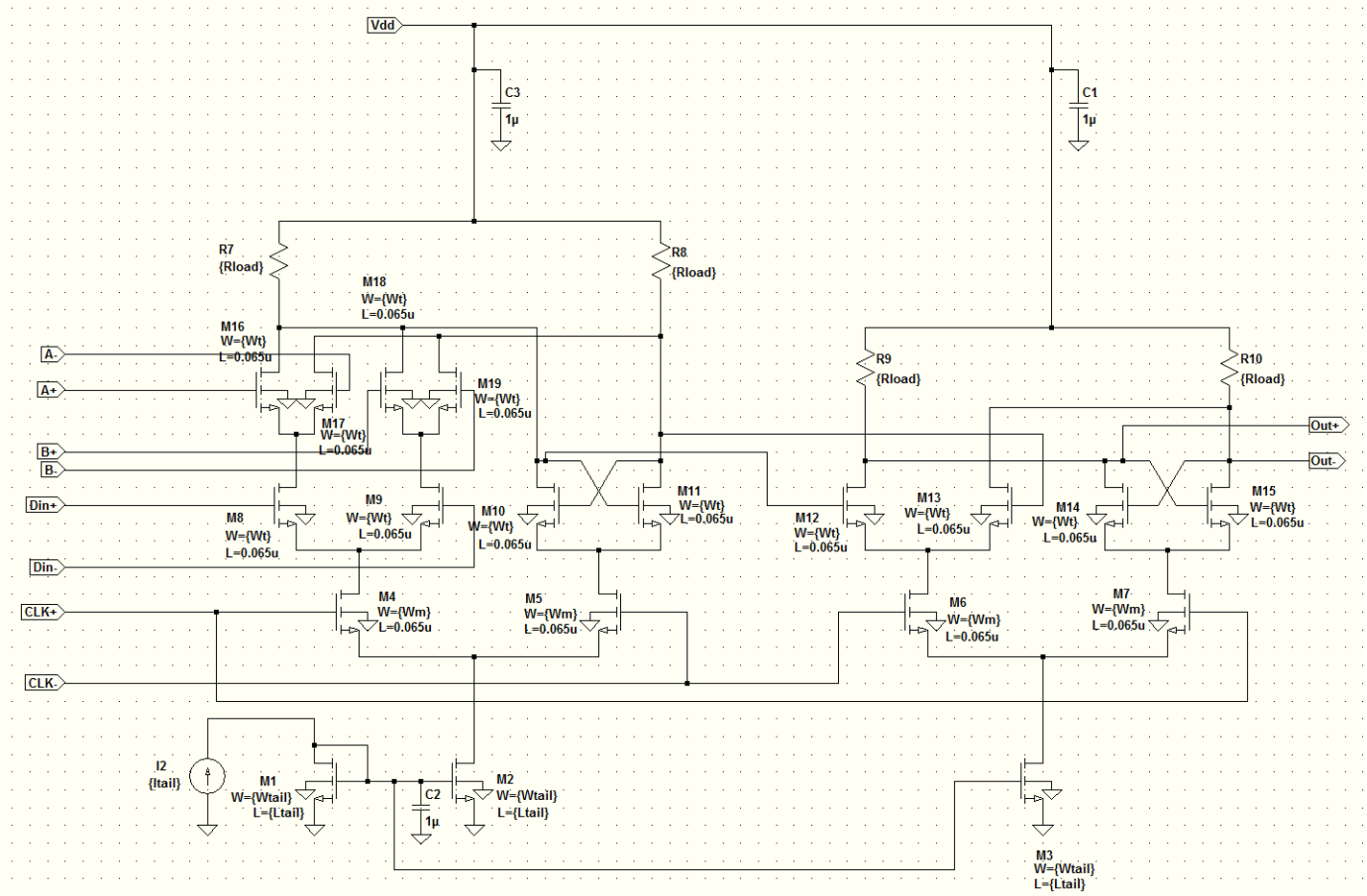
- D Flip Flop in /2 configuration with merged AND gate
- 2 input OR gate

Sub-block: Modulus 2/3 Prescaler – Schematic

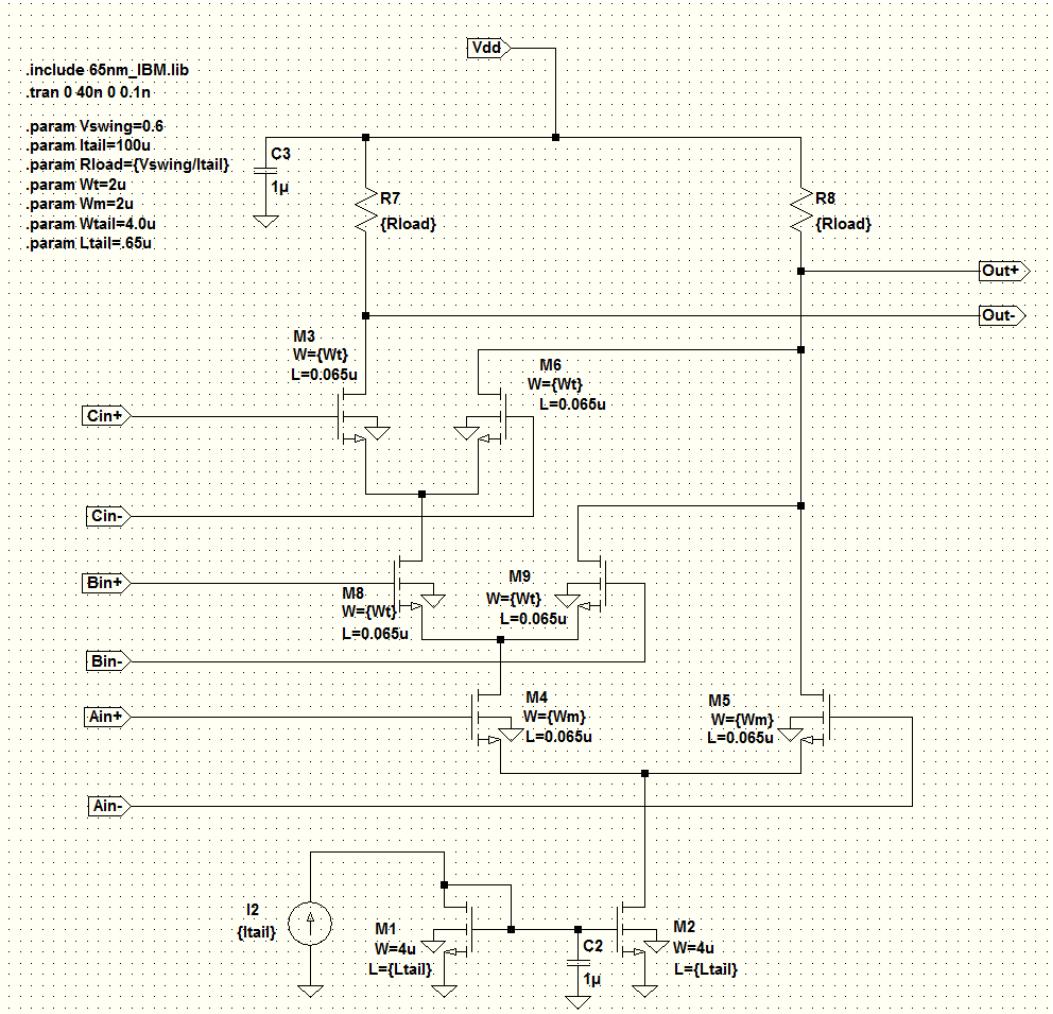


- AND gate is merged into FF3 sub block
- 3 input OR gate is not merged

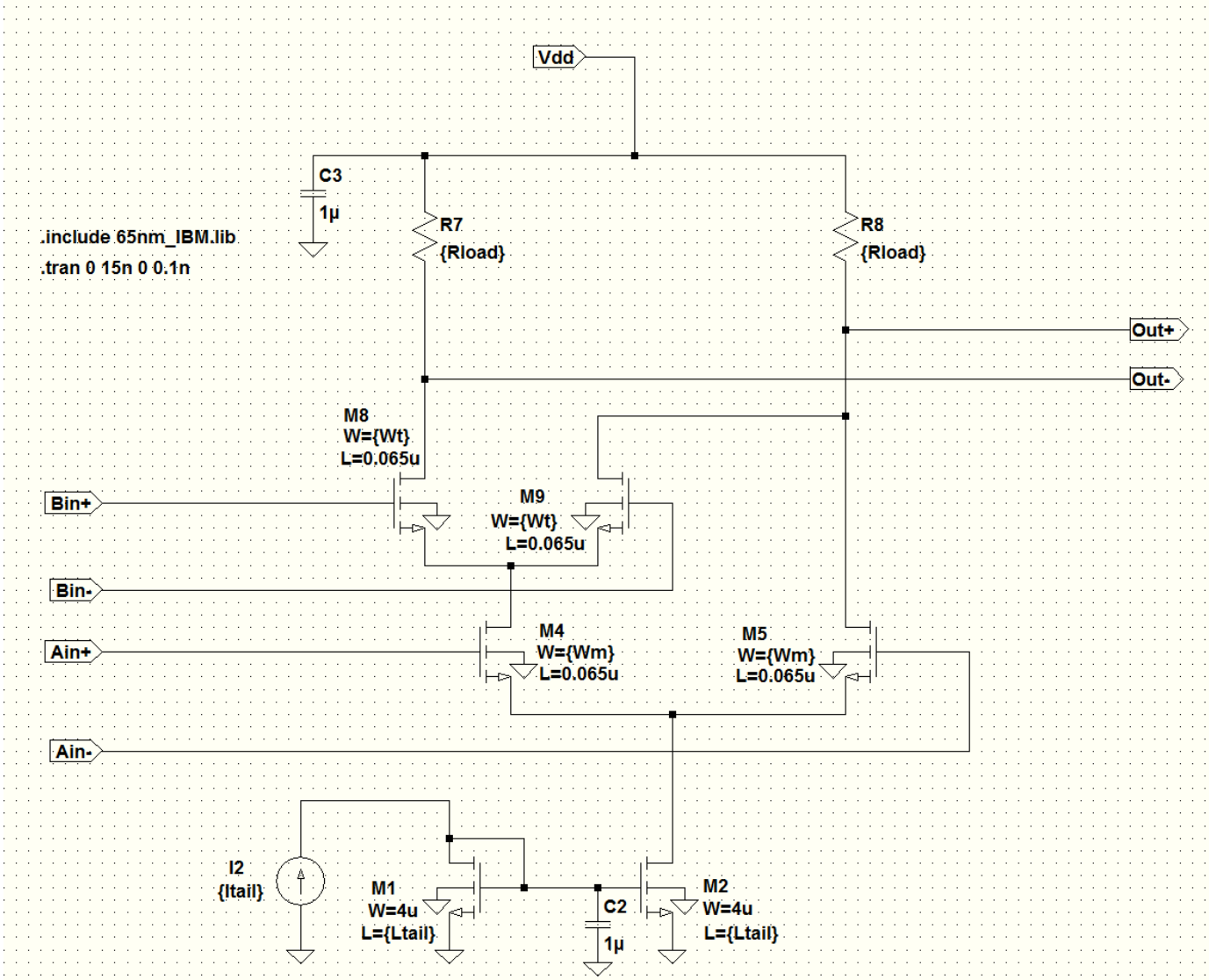
D Flip Flop with Merged AND gate



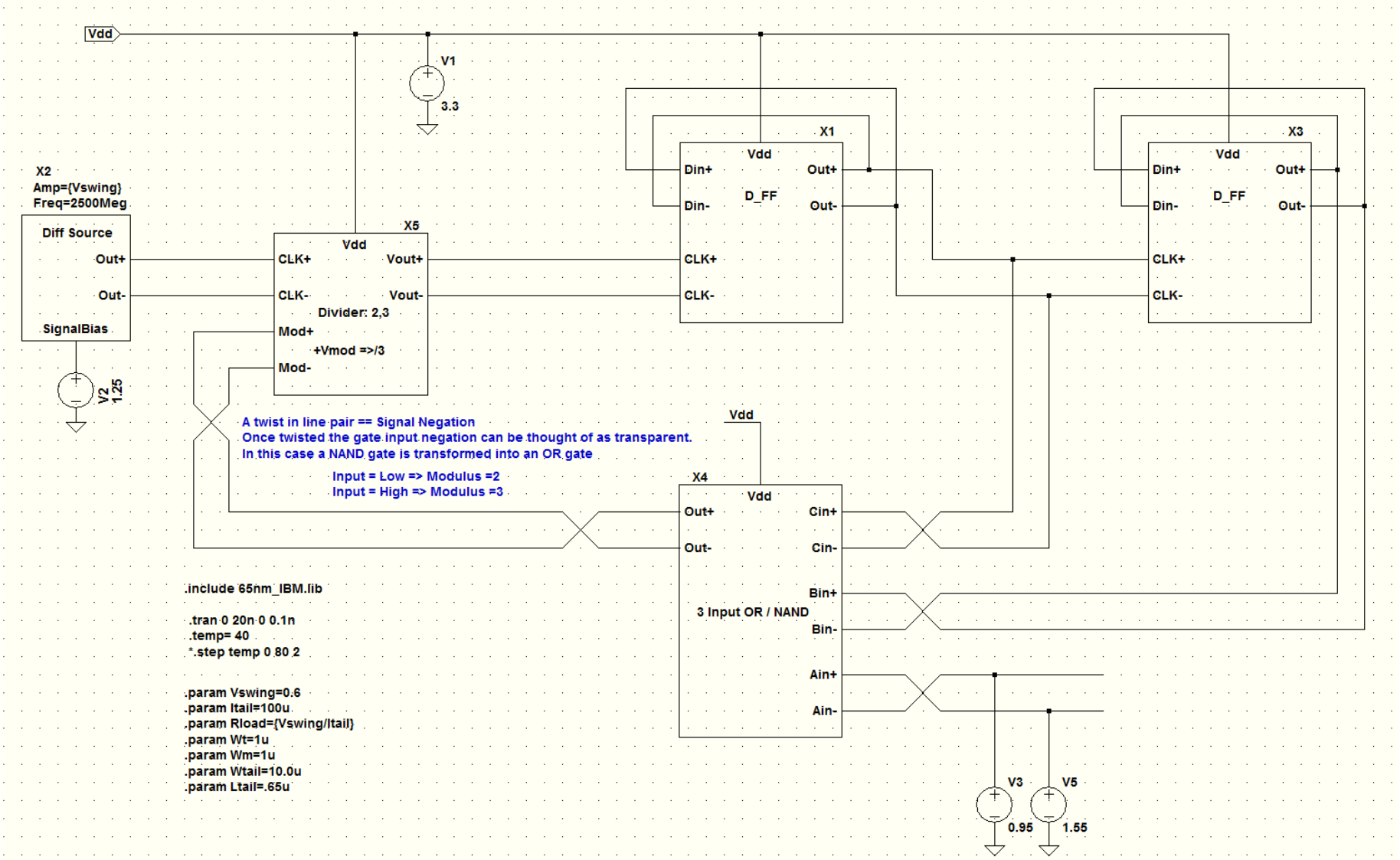
Block : 3 Input OR gate



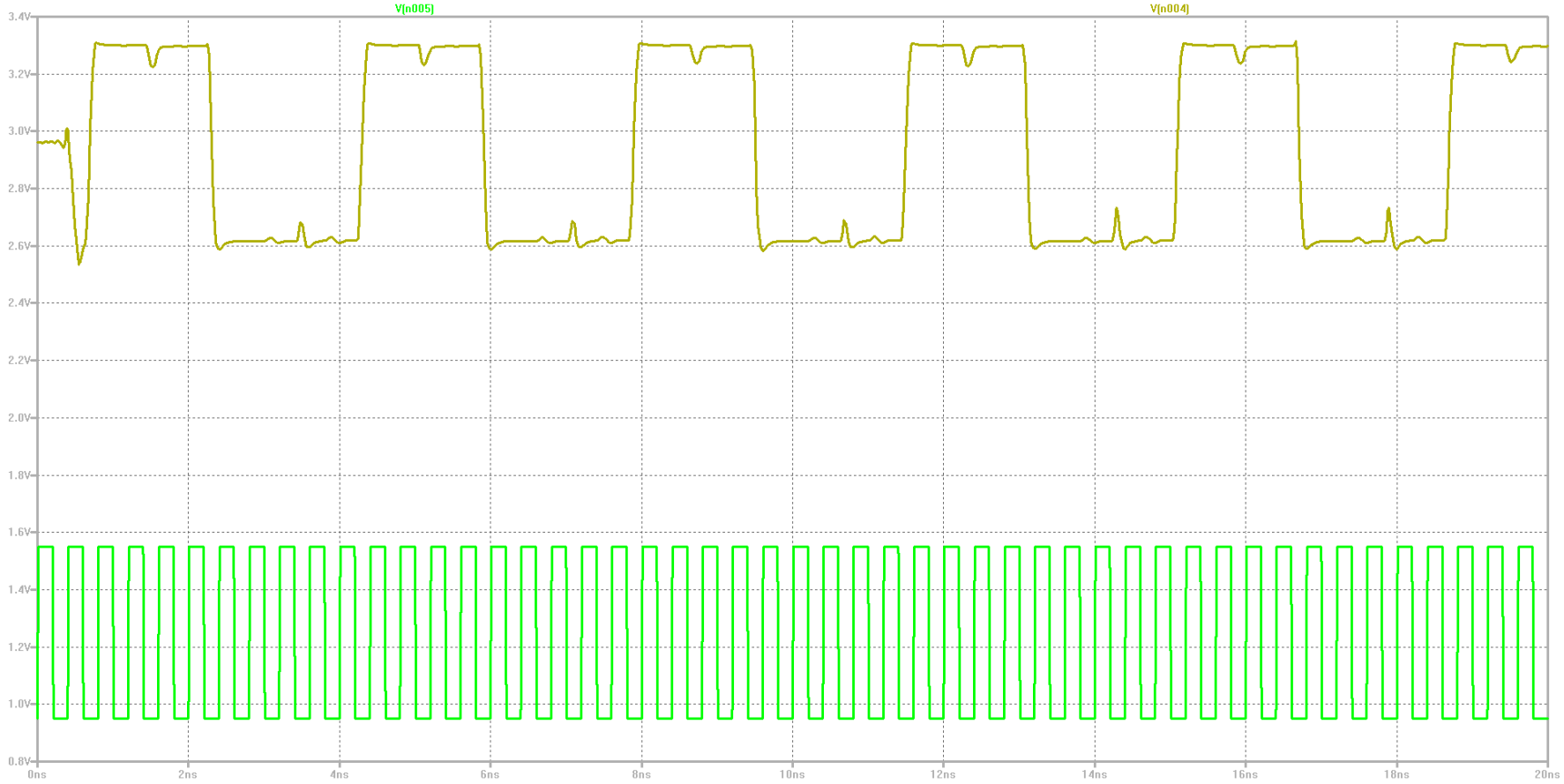
Block : 2 Input OR gate



Modulus = 8/9 Prescaler Schematic

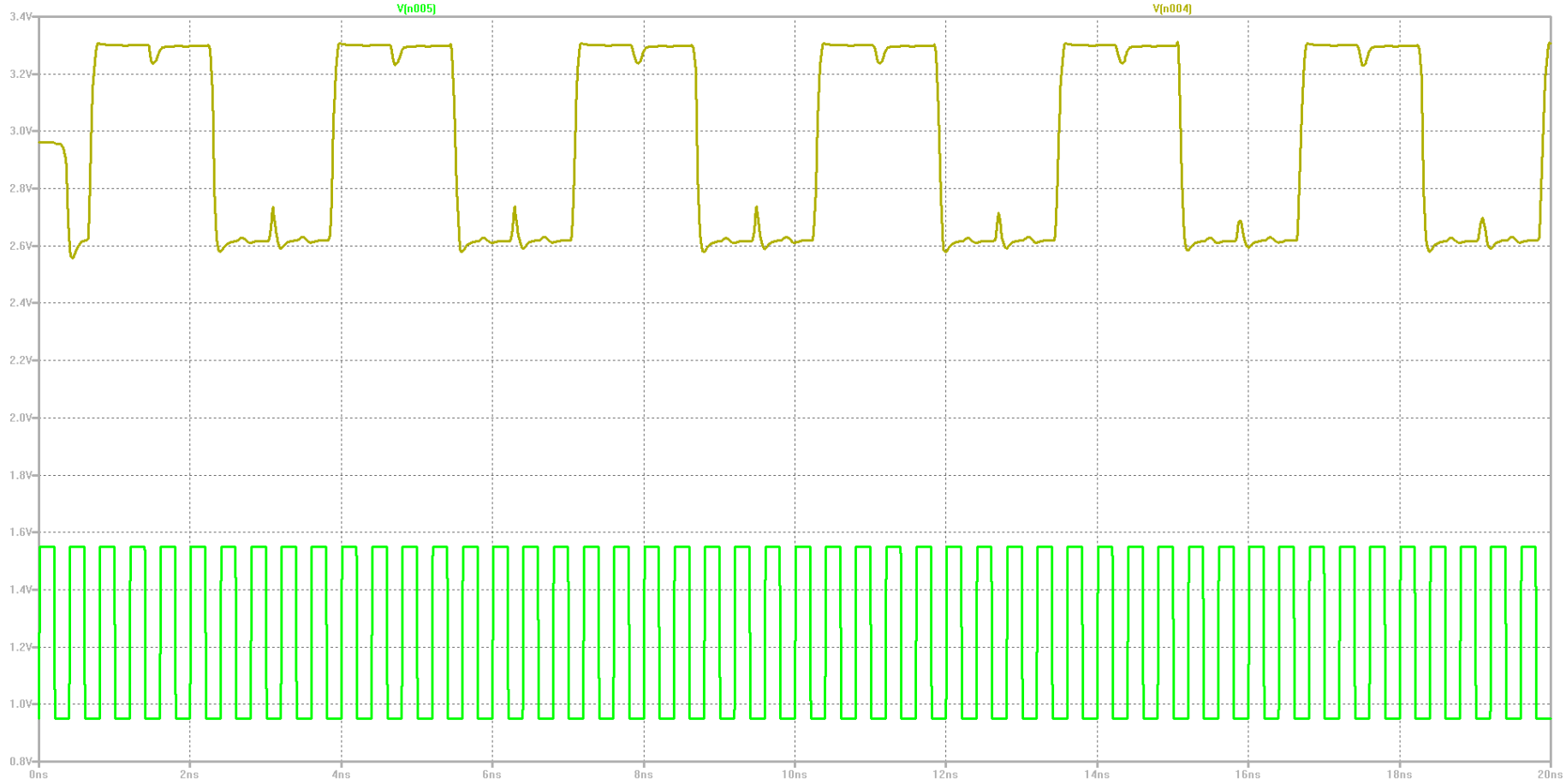


8/9 Prescaler with MOD=9



- Input Frequency = 2500MHz

8/9 Prescaler with MOD=8



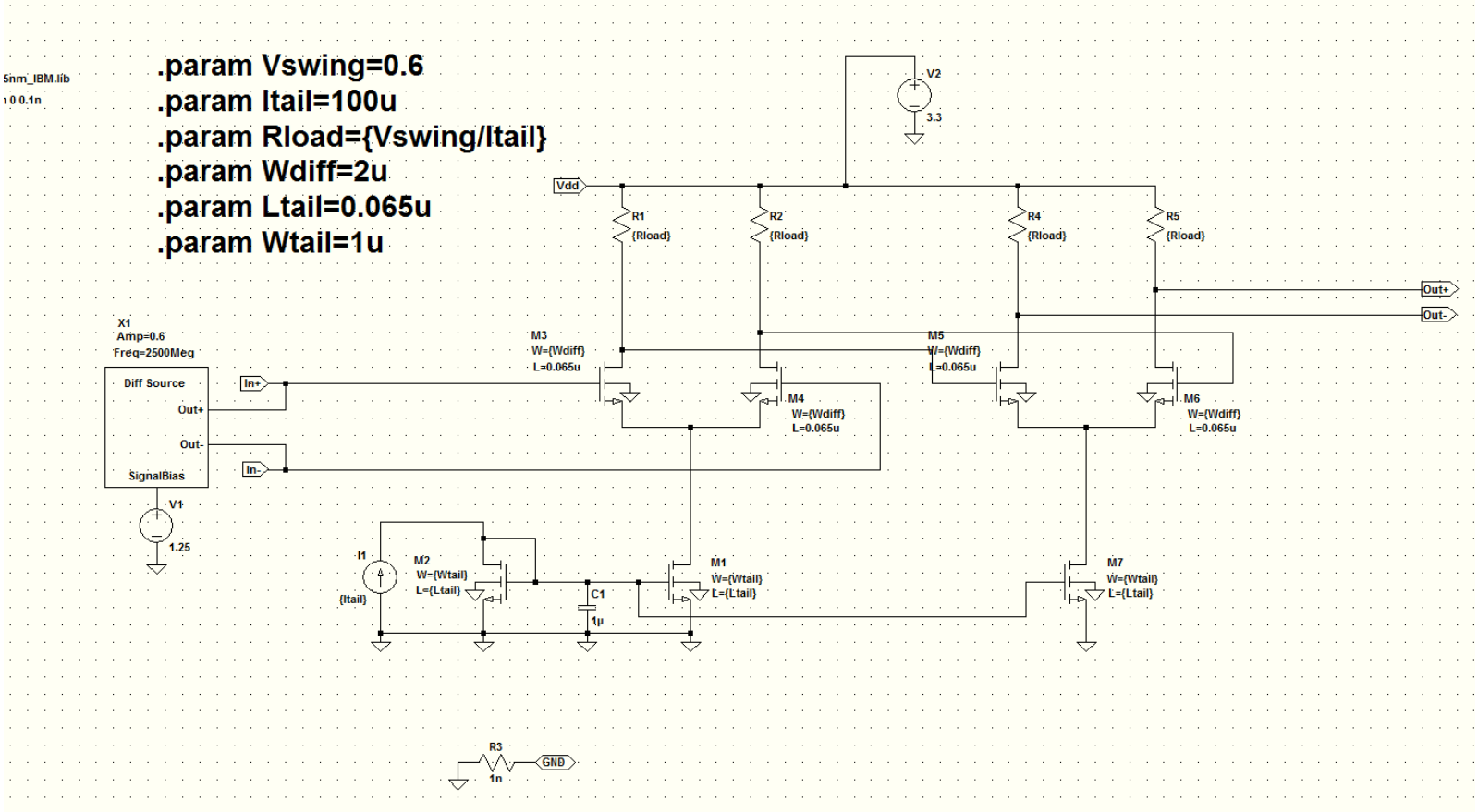
- Input Frequency = 2500MHz

Input Differential Amplifier

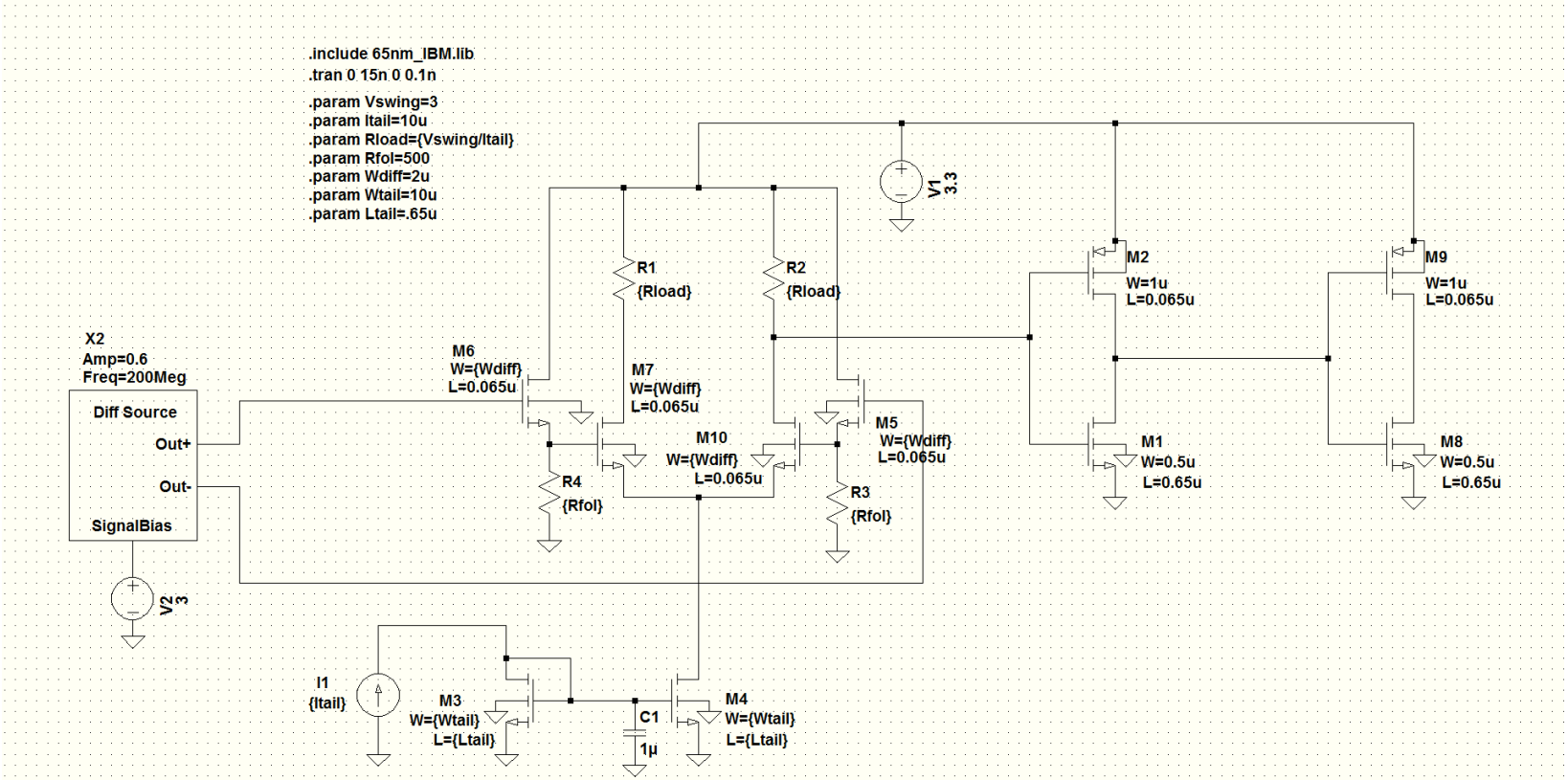
•Diff Amp with MOSFET differential amplifiers –BiCMOS would be much better according to the papers. To square up the input signal requires too many stages with MOSFETs

•Same current tail MOSFET dimensions were tried but did not work well. Simulation suggested a much smaller set of dimensions

•You need at least 2 stages to get a nice flat top and bottom. This is because the 3.3 V rail gives good limiting. With signal inversion both top and bottom of signal end up flattened.

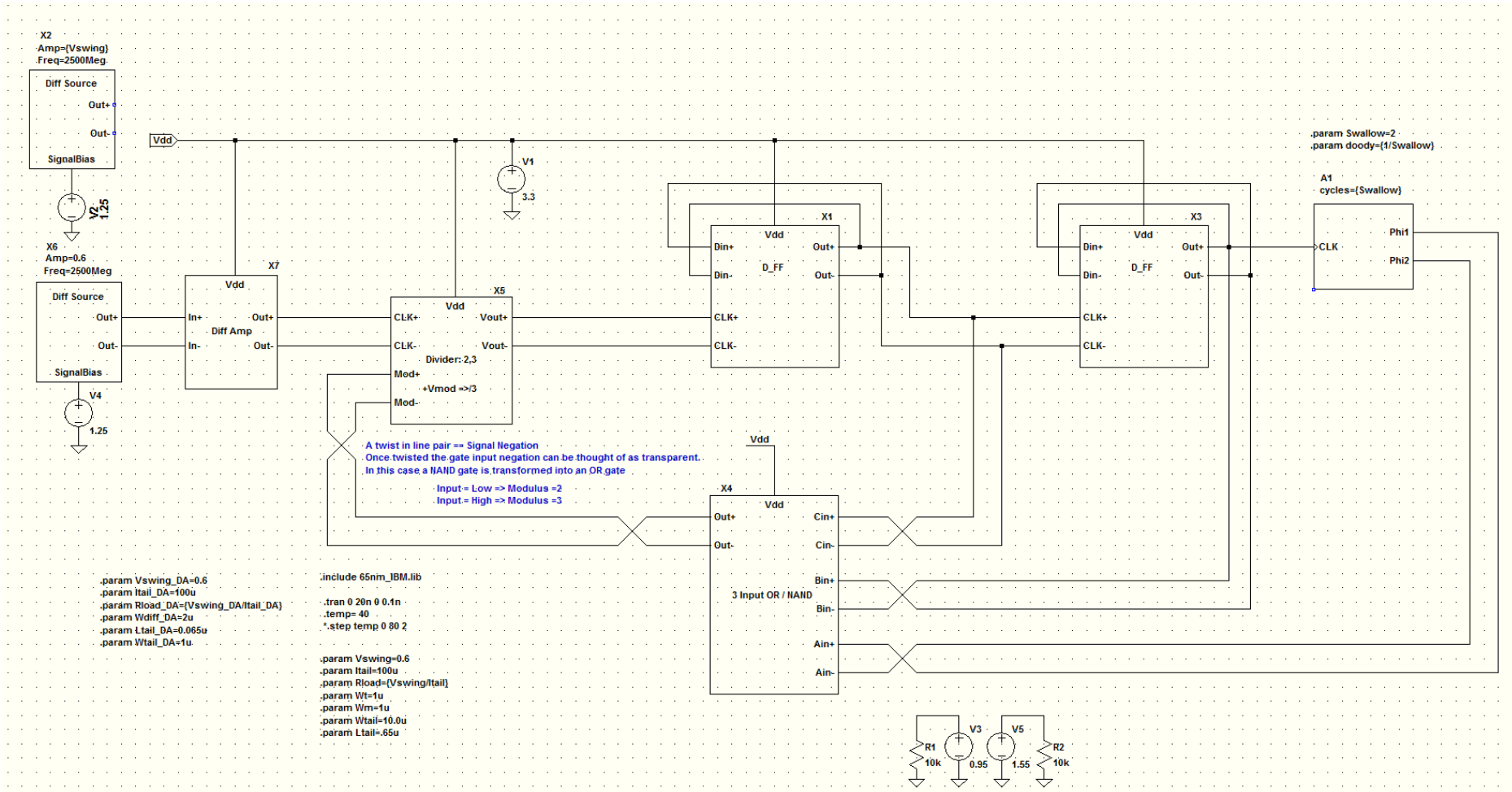


CML to CMOS Converter

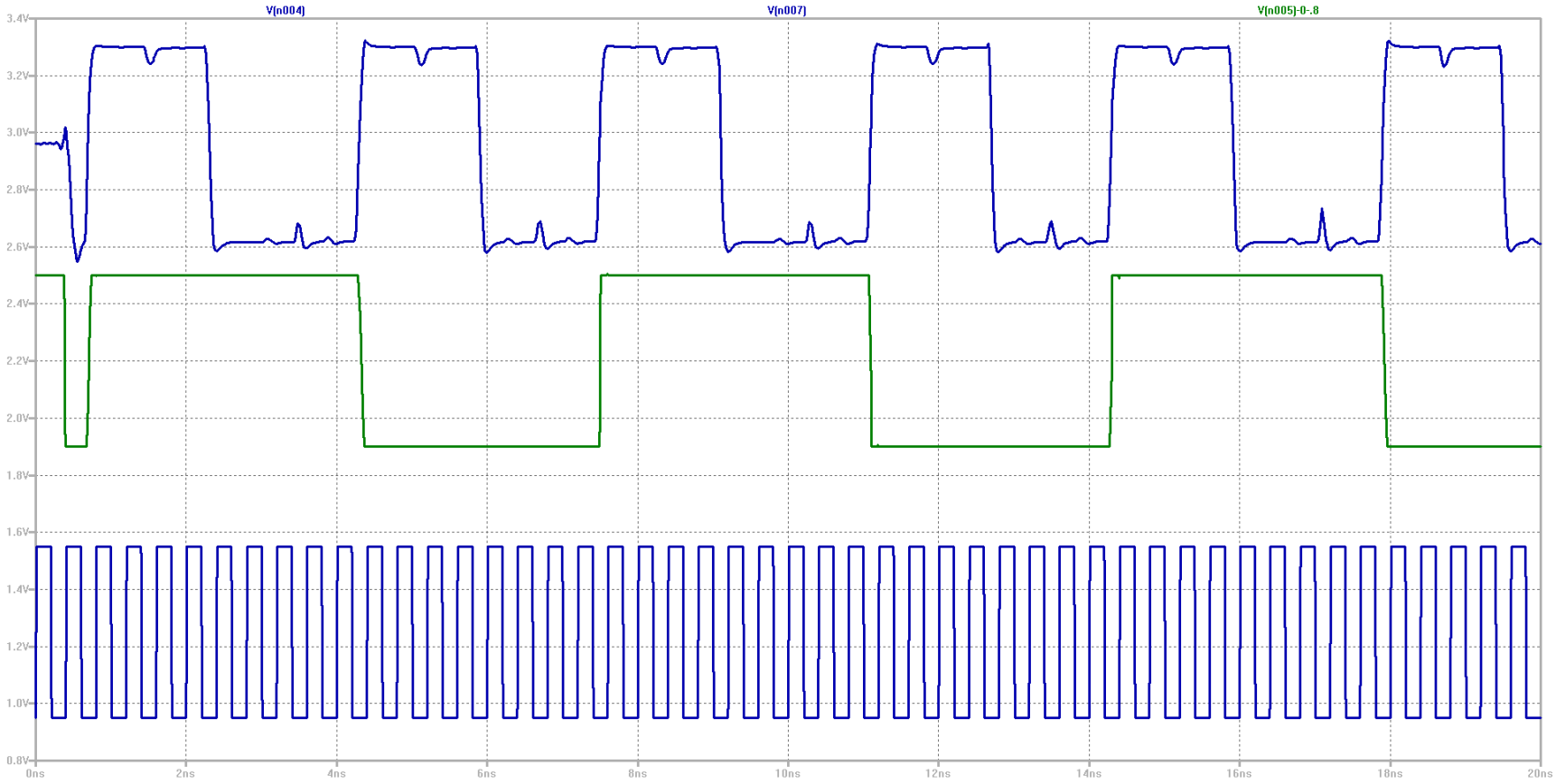


- Same MOSFET dimensions for differential pair and level shifters – same reasoning.
- Requires level shifters on the diff pair input float the source and drain voltages down to accommodate the input of the CMOS inverter
- 1st Inverter is not fully driven and a second stage is required
- Rload=7.5
- Itail=400uAmp – higher current required to get the drop without increasing R too much

Behavioral Schematic



Behavioral Simulation



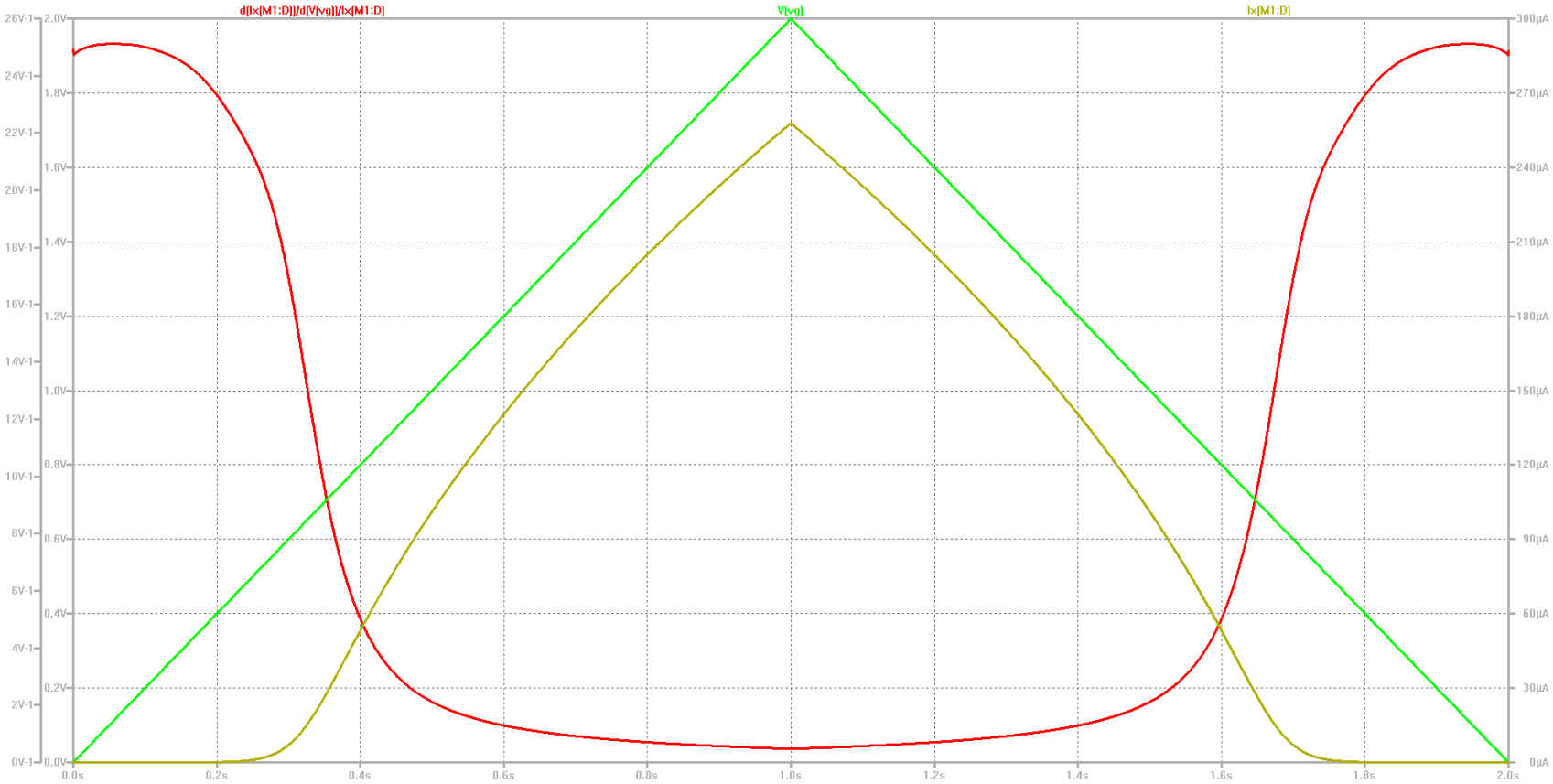
- Traces: Prescaler Out, Modulus Control, Fin=2500MHz
- Prescaler feeds /2 counter that controls the modulus input of the prescaler
- Division ratio thus alternates between /8 and /9 for each pulse out of the prescaler
- Works good at this frequency

Operational Envelope

- Frequency Limit: 5GHz @ 25 deg C => dual modulus stops working
  - 4GHz worst case over -40 to +80 deg C
- Input signal magnitude: 50mV pp @ 25 deg C
- Supply Voltage over -40 to +80 deg C
  - Minimum=3V
  - Maximum=3.5V
- Power consumption = Vdd * Itail * NumTails = 5mW total
- Temperature Range: -40 to 110 deg C with
  - Vpp-in=0.2V
  - nom Vdd
  - Fin=2500MHz

Appendix 01

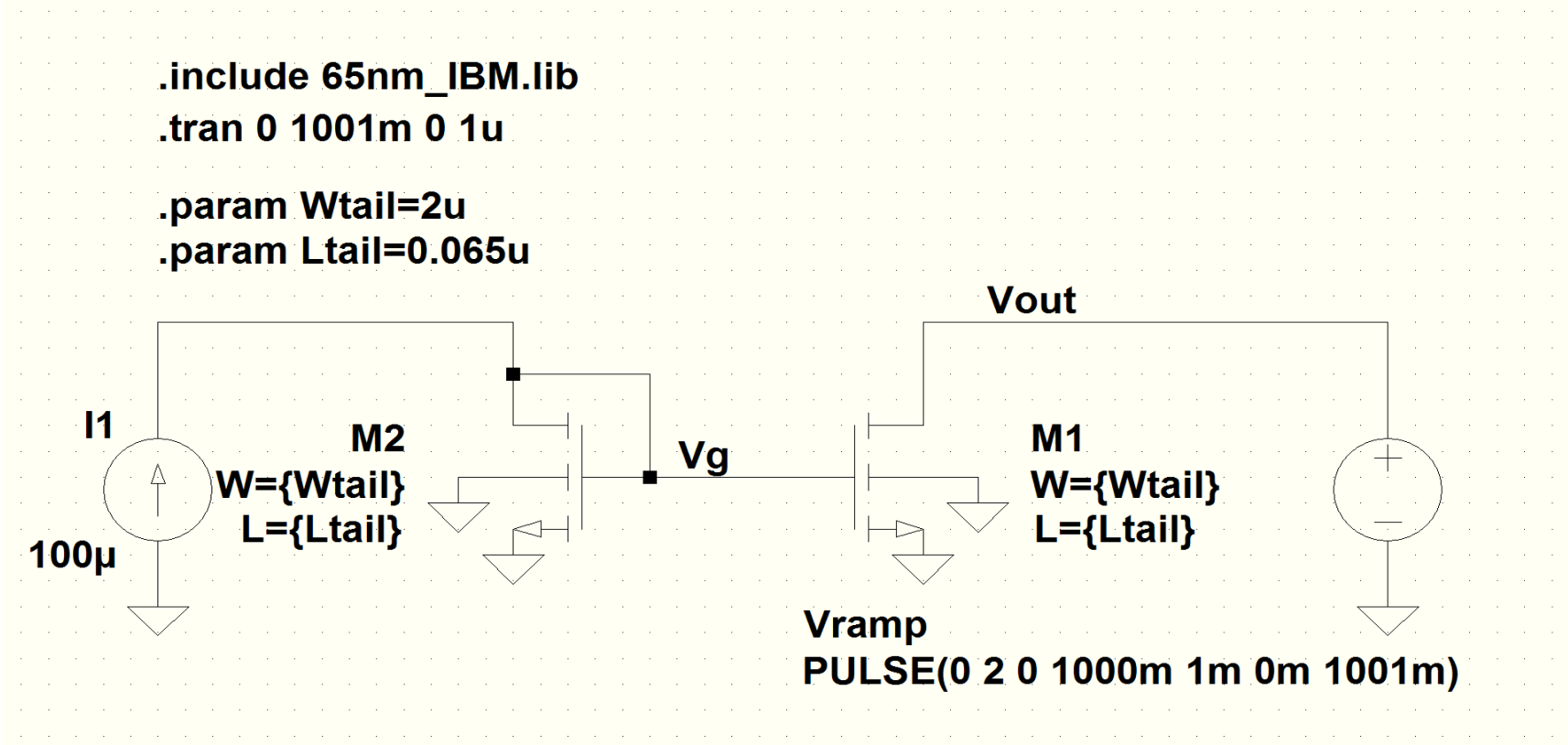
NMOS Specific Current of W=1uM,L=Lmin MOSFET



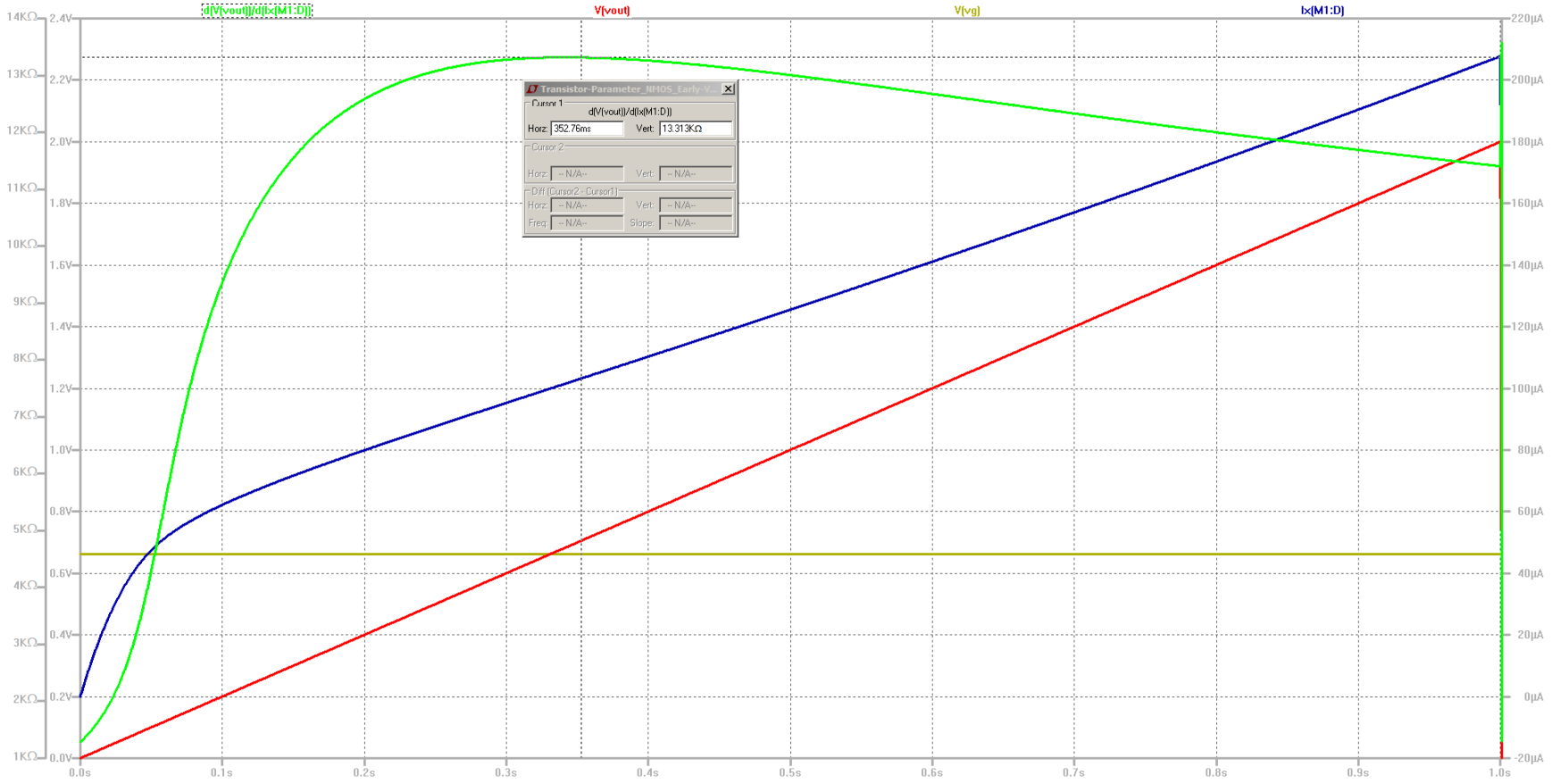
- Ispecific = 2uAmp
- Vt=0.650
- N=1.6 slope factor

Curves are: Vgate, Idrain, gm/Id

Appendix 02: Early Voltage

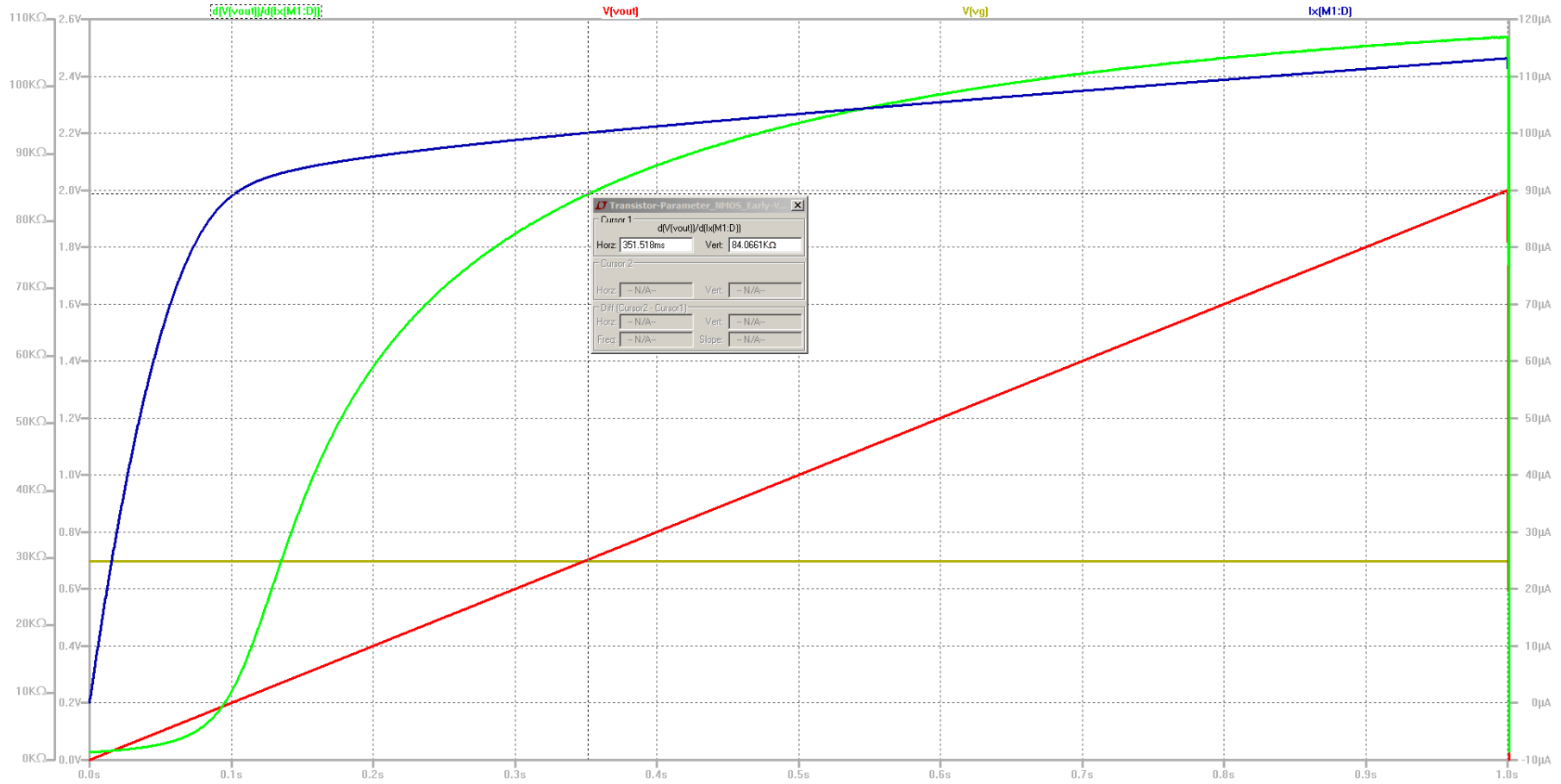


Signal FET: W=2uM, L=Lmin



With Vdrain 0.350V or greater Rdrain=~13kOhm

Tail FET: W=10uM, L=10*Lmin



Rdrain=85kOhm @ 0.350 V

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