Pulse swallowing frequency divider with low power and compact structure*

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Abstract: A pulse swallowing frequency divider with low power and compact structure is presented. One of the DFFs in the divided by 2/3 prescaler is controlled by the modulus control signal, and automatically powered off when it has no contribution to the operation of the prescaler. The DFFs in the program counter and the swallow counter are shared to compose a compact structure, which reduces the power consumption further. The proposed multi-modulus frequency divider was implemented in a standard 65 nm CMOS process with an area of 28 × 22 μm^2. The power consumption of the divider is 0.6 mW under 1.2 V supply voltage when operating at 988 MHz.

Key words: frequency divider; low power; prescaler; multi-modulus; CMOS

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1. Introduction

The phase-locked loop (PLL) is a critical block in modern wireless communication systems, which usually consist of a voltage controlled oscillator (VCO), a frequency divider, a frequency-phase comparator, and a low pass filter. Although the speed of the RF building blocks increases with process improvement, power consumption is still a bottle-neck for the long battery lifetime of the system. The frequency divider and VCO operate at the highest frequency and dominate in the power consumption of the PLL. Due to the divider's complexity, low-power design of the divider becomes more critical than that of the VCO.

Previous papers have been presented focusing on the implementations of low power D flip-flops and low power dividers. In Ref. [1], a new current mode logic (CML) D-latch that integrates the dynamic configuration is proposed; it optimizes the performances in the power consumption, output voltage swing and operating frequency. In Ref. [2], a mono-stable circuit is inserted between the input signal and the D-latch; the proposed mono-stable frequency divider significantly minimizes the number of switching transistors and thus reduces the dynamic power dissipation. In Ref. [3], "time reuse" technique is proposed to reduce the delay of the phase-switching control loop and power supply voltage can be reduced. In Ref. [4], a novel D-latch integrated with an "OR" logic gate is used to optimize the power consumption.

In this paper, a pulse swallowing frequency divider with low power and compact structure is presented. The working state of the conventional pulse swallowing frequency divider was analyzed and a new architecture with DFF powered off and DFFs shared was proposed for lower power consumption.

2. Low power MMD design

2.1. Conventional MMD analysis

Figure 1 shows the block diagram of a conventional multi-mode divider (MMD) based on a dual-modulus prescaler, a program counter and a swallow counter. Figure 2 shows the corresponding time diagram ($N = 2$, $P = 7$, $S = 4$). When the circuit begins from the reset state, the prescaler divides F_{in} by $N+1$. The output of the prescaler is divided by both the program counter and swallow counter until the latter is "full". At this point, the swallow counter changes the state of the modulus control line, making the prescaler divide F_{in} by N. After this, the prescaler and the program counter continue to divide until the latter is "full". The state of MMD is reset by the reset signal and another period of division begun.

2.2. Low power divided-by-2/3 prescaler

A divided-by-2/3 prescaler comprises two latches with AND/OR gates as shown in Fig. 3(a). When MC = 1, the divider operates at divide-by-3 mode, and one extra period of the input signal is swallowed by latch2. When MC = 0, the divider operates at divide-by-2 mode. In this mode, the output of latch2 keeps low and has no extra contribution to the operation of the whole prescaler. Figure 3(b) shows the time diagram of internal nodes in latch2 when MC = 0. Although the QB output of latch2 keeps high, charging and discharging occur at some

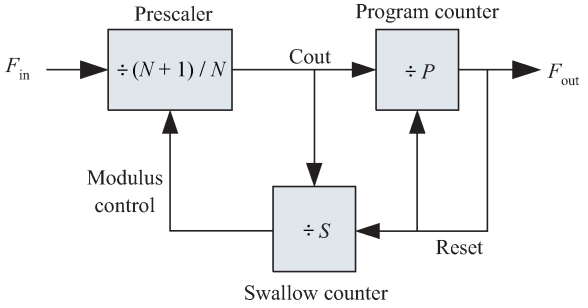

Fig. 1. Structure of a conventional MMD.

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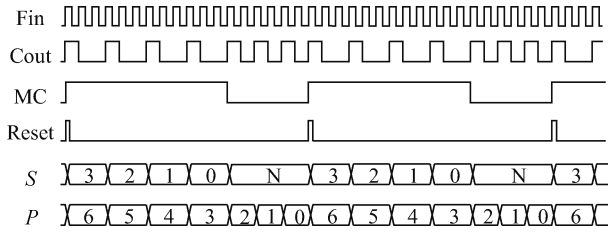

Fig. 2. Time diagram of conventional MMD ($N = 2$, $P = 7$, $S = 4$).

internal nodes such as S2 and S3, causing dynamic power consumption.

Figure 3(c) shows the proposed low power divide-by-2/3 prescaler with latch2 powered off when MC = 0. Transistor MN1/MP1 are added to latch2 and controlled by the mode control signal MC. When MC = 1, MN1 is turned on and MP1 is turned off, latch2 performance the same function as latch1, the divider operates at divide-by-3 mode. When MC = 0, MN1 is turned off and MP1 is turned on, the internal nodes S2/S3 keep high and output node Q keeps low, the divider operates at divide-by-2 mode and the dynamic power consumption of latch2 is eliminated. Figure 4 shows the simulated current wave form of the proposed and conventional divided by 2/3 cell. It can be seen that the power is reduced drastically in the divided-by-2 mode.

2.3. P/S counters with shared DFFs

In the conventional MMD, the swallow counter is idle after S periods of C_{out} until the reset signal become high, as shown in Fig. 2. The proposed method above can be used to power off the DFFs in the swallow counter when MC = 0 for low power design, but the parasitic capacitor associated with the DFFs are still load the prescaler heavily and increases the power of the prescaler.

Figure 5(a) shows the proposed P/S counter with DFFs shared. It consists of a down counter (DC), a logic comparator, an NOR gate and an output DFF. The inputs are F_{in}, $P[n]$, $P[n] - S[n]$, the outputs are MC and F_{out}. The DC is a programmable down counter starting from $P[n]$, its output is fed into the logic comparator (shown in Fig. 5(a)) and the NOR gate. The logic comparator compares the counting result $C[n]$ with $D[n] = P[n] - S[n]$ and the output keeps low until the two inputs are equal. After $S[n]$ periods of F_{in}, $C[n] = P[n] - S[n]$, the output of the logic comparator changes from "0" to "1" and produces a "rise-edge" to trigger the output DFF and MC becomes high. This logic process behaves the same as that of the conventional S counter. The output of the NOR gate serves as the reset signal. After P[n] periods of F_{in}, $C[n] = 0$, Reset become high. The down counter is reloaded and the output DFF is reset, DC counts starting from $P[n]$ and MC become low. This logic process behaves the same as that of the conventional P counter.

From the above analysis, it can be concluded that the function of the proposed counter is the combination of that of the swallow counter and the programmable counter. Since the number of DFFs is reduced, the power consumption of the proposed counter is less than the total power consumption of the swallow counter and the programmable counter. Furthermore, the capacitive loading to the output node of the prescaler generated by the proposed counter is also reduced compared with that generated by both the swallow counter and the programmable counter, so the power consumption of the prescaler can also be reduced drastically.

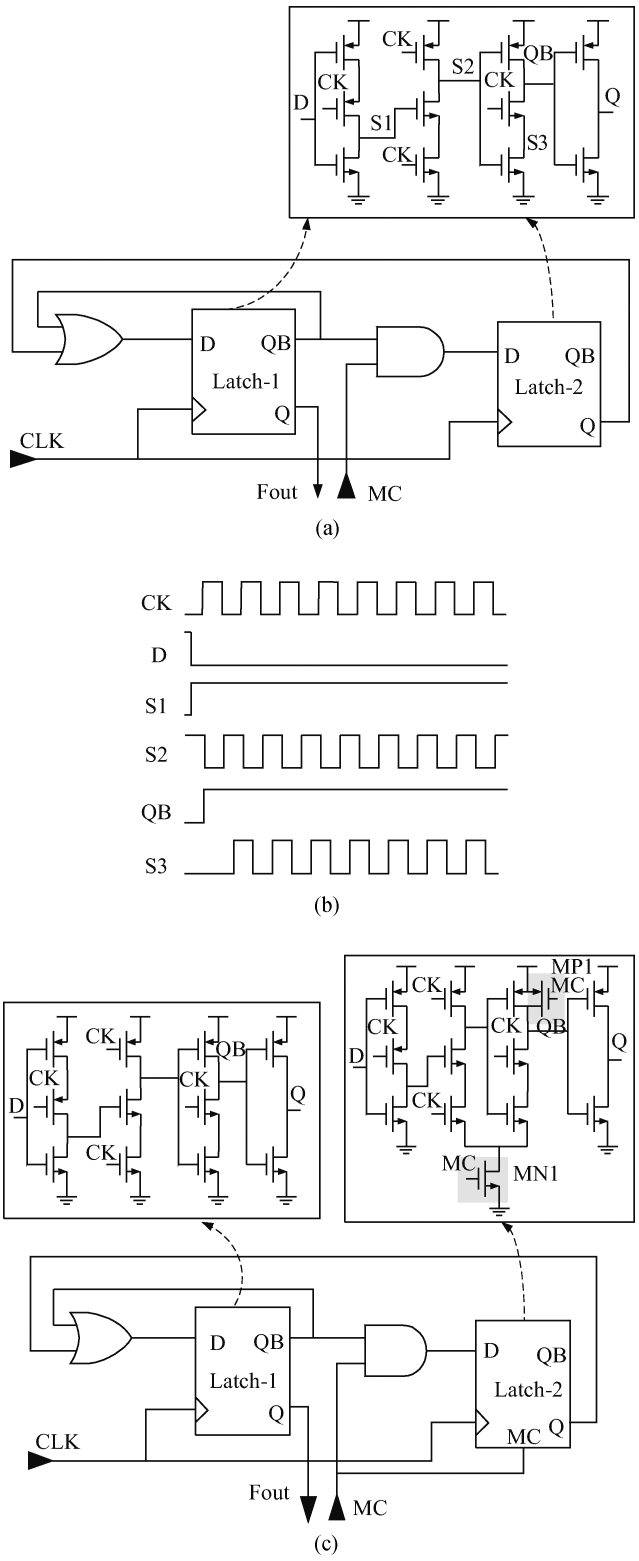

Fig. 3. (a) Structure of the prescaler. (b) Time diagram of internal nodes in latch2 when MC = 0. (c) Proposed prescaler with latch2 powered off when MC = 0.

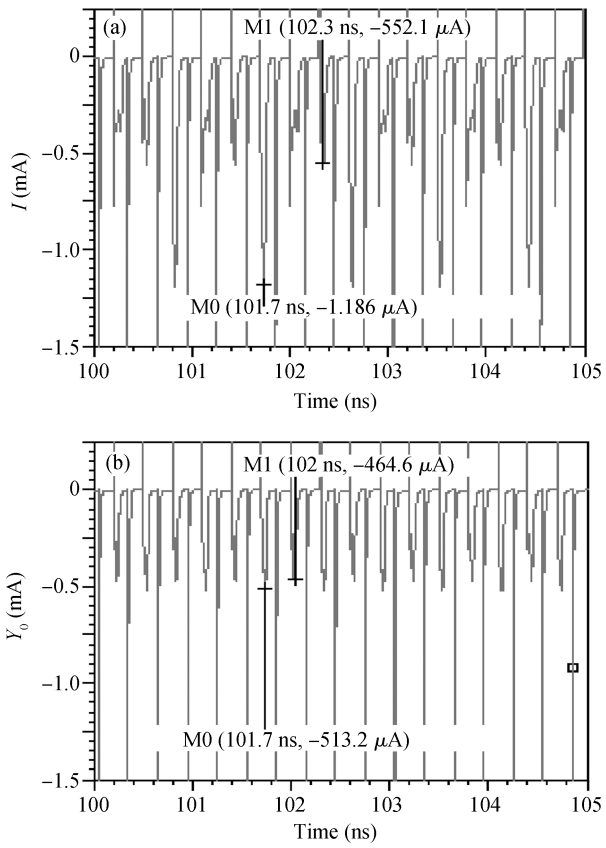

Fig. 4. Simulated current wave form of (a) the proposed and (b) conventional divided by 2/3 cell.

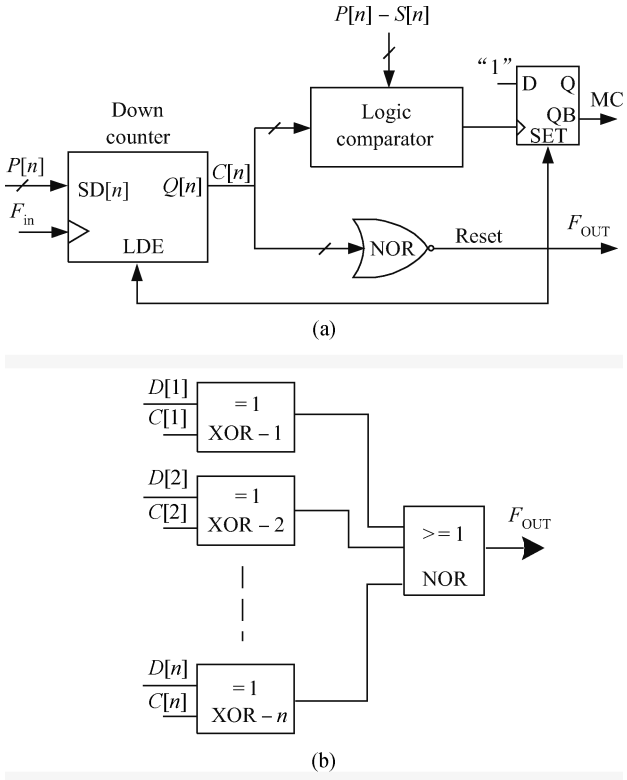

Fig. 5. (a) Structure of the proposed P/S counter. (b) Structure of the logic comparator.

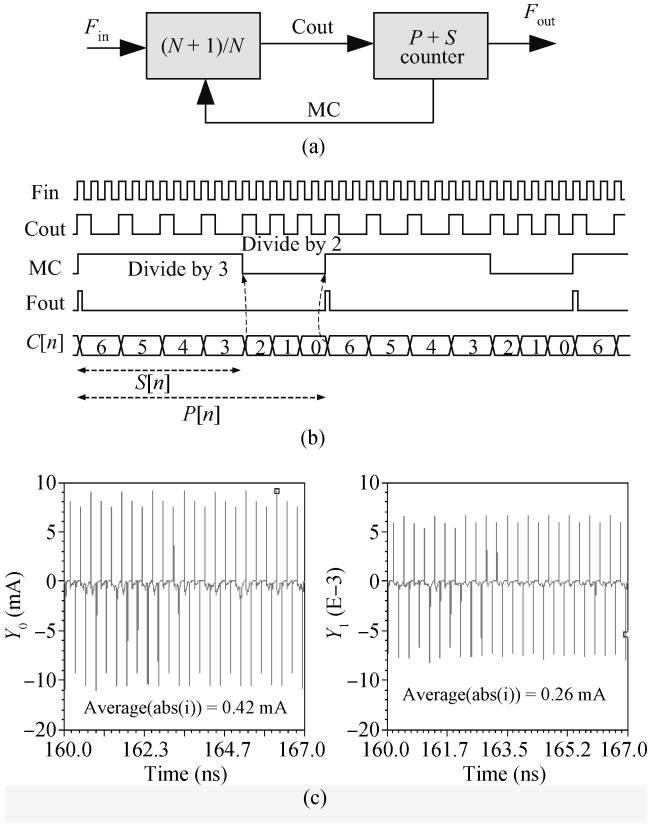

Fig. 6. (a) Structure of the proposed divider. (b) Time diagram of the proposed MMD ($N = 2$, $P = 7$, $S = 4$). (c) Current wave forms of the proposed (right) and conventional (left) pulse swallowing counter ($N = 2$, $P = 7$, $S = 4$).

2.4. Pulse swallowing frequency divider design

The structure of the pulse swallowing frequency divider with low power is shown in Fig. 6(a). It consists of a divided-by-2/3 prescaler and $P + S$ counter. The power saved for the prescaler depends on the value of P and S[5]. The minimum saved power is 12.5% When $P = 3$, $S = 2$. For maximum power reduction, the P should be as large as possible and the S should be as small as possible. With the $P + S$ counter, nearly 50% power can be saved compared with that of conventional P/S counter. Moreover, due to the reduction of the parasitic capacitance loading the prescaler, extra power can be saved for the prescaler. Figure 6(b) shows the time diagram of the proposed multi-modulus divider ($N = 2$, $P = 7$, $S = 4$). Compared with that of the conventional one shown in Fig. 2, it can be seen that the function is unchanged. Figure 6(c) shows the simulated current wave forms of the proposed (right) and conventional (left) pulse swallowing counter when $N = 2$, $P = 7$, $S = 4$. It can be seen that 38% of the power is saved.

3. Implement and measurement results

The proposed divider was designed and implemented in SMIC 65 nm CMOS process. Figure 7 shows the layout and the micrograph of the divider, the die area is 28×22 μm^2.

Due to the limitation of the pad, only the output of the prescaler is drawn forth for test purpose and the input signal is fed by the on-chip ring oscillator. Figure 8(a) shows the output

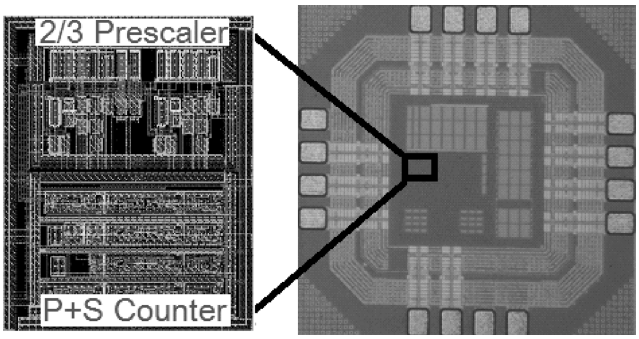

Fig. 7. Layout and the micrograph of the divider.

spectrum of the prescaler in divide-by-2 mode when the frequency of ring oscillator is set at 1009 MHz. The function of the whole divider is verified through the locking action of the PLL. Figure 8(b) shows the output spectrum of the PLL when locked at 988 MHz, the power consumption of the divider is 0.6 mW under 1.2 V supply voltage at this case. Figure 8(c) shows the power consumption of the divider versus division ratio when the PLL is under lock. As division ratio increases, the power consumption of the conventional divider increases more rapidly than that of the proposed divider, this is due to the reduction of switching activity by reduced number of DFFs in the proposed divider.

4. Conclusion

A low power pulse swallowing frequency divider was demonstrated in 65 nm CMOS process. The DFF in the prescaler is controlled by the mode controlling signal and powered off in the idle state, the DFFs in the program counter and swallow counter are shared, thus power consumption is reduced. The experimental results show large power reduction is achieved by the proposed divider. We can conclude that the proposed divider is well suitable for low power design.

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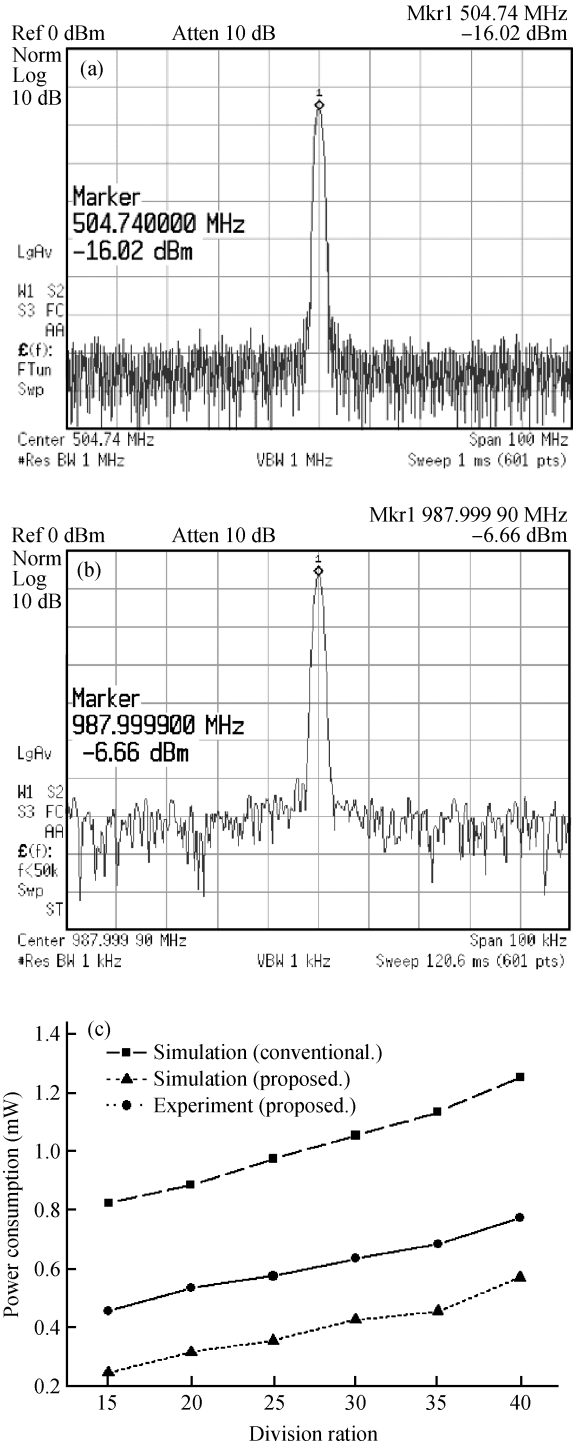

Fig. 8. (a) Measured output spectrum of the divider. (b) Output spectrum of the PLL when locked. (c) Measured power consumption versus division ratio.

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