A 1.8V, 3GHz 16/17 Dual Modulus Prescaler in 0.35μm CMOS Technology

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Abstract — *A dual-modulus (divide-by-16/17) prescaler has been designed using a 0.35μm CMOS technology. It consists of a divide-by-4/5 synchronous divider and a divide-by-4 asynchronous divider, all implemented with MOS current mode logic. The operating frequency range is simulated to be from 0.8 to 3.1 GHz including all parasitics. The prescaler including the output buffers driving external 50Ω load draws about 14mA from a 1.8V power supply.*

I. INTRODUCTION

The frequency synthesizer are one of the most critical parts in a wireless transceiver. Most frequency synthesizers are of the phase-locked loop (PLL) type [1], as shown in Fig. 1. In the frequency synthesizer, only the VCO and prescaler operate at the highest frequency. It is relatively easy to design a multi-gigahertz voltage controlled oscillator (VCO) in the current advanced CMOS process, so the dual modulus prescaler remains the most critical components with the trend of applying CMOS into higher frequency systems.

Operating at the highest frequency, the dual modulus prescaler divides the output frequency of the VCO by one of the two fixed division ratios to a lower frequency. This division ratio is controlled by a modulus control signal generated by the programmable counter. Besides the high operating speed, the dual modulus prescaler also has to be efficient in terms of current consumption, and be able to work at low supply voltage.

In this paper, we present a 16/17 dual-modulus prescaler operating up to 3.1GHz realized in a 0.35μm CMOS technology with 1.8V supply voltage. By merging NAND logic with D-flip-flop, we eliminated their propagation delay. Also, by merging AND logic that counts asynchronous output into flip-flop with NAND logic, it allowed are accurate pulse swallow by eliminating the delay that was found in the AND logic.

In Section II, conventional dual modulus prescaler is described. The new fast dual modulus prescaler is described in Section III. Section IV shows HSPICE simulation results and then the conclusion follows in Section V.

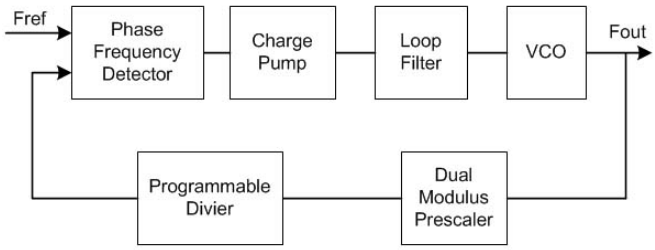


Fig. 1. Block diagram of PLL frequency synthesizer

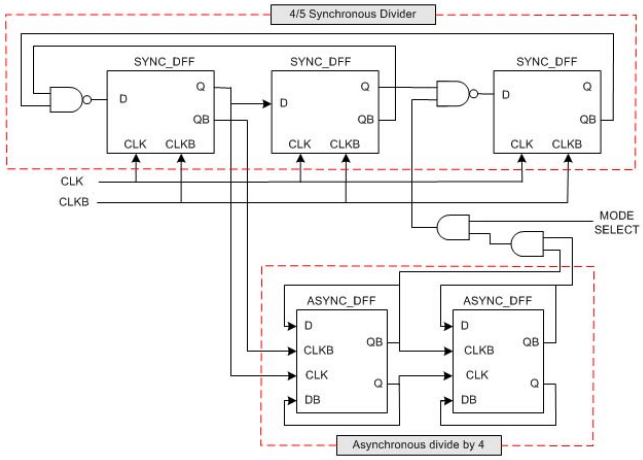


Fig. 2. Block diagram of the conventional dual modulus prescaler

II. CONVENTIONAL DUAL MODULUS PRESCALER

Fig. 2 is a block diagram of the conventional 16/17 dual modulus prescaler.

A synchronous counter is composed of three D-flip-flops (F/F) and two NAND gates, and an asynchronous counter is composed of two D-F/F's. The operating frequency of the asynchronous counter is one-fourth or one-fifth of the synchronous counter according to the MODE select signal. Therefore, F/F's in the asynchronous counter can be designed to draw less current than the one used in the synchronous counter.

The maximum operation frequency of a prescaler is determined by the synchronous counter because it is clocked at the highest frequency. Since the synchronous counter is composed of three D-F/F's and two NAND gates, the maximum operating frequency of the dual modulus prescaler is determined by the propagation delay of the NAND gates and the F/F's in the synchronous counter.

Some design techniques have seen proposed recently among which the merged structure of NAND gate and D-F/F is the most popular one [2-3]. Merging the F/F with the series-connected NAND logic as shown in Fig. 3 has the effect of eliminating the delay of NAND gate and thus enables faster operation.

However, because a NAND gate has series-connected transistors, this structure has double effective resistance and slower current switching speed, compared with one transistor having the same size. Therefore, in order to decrease the effective resistance, we implemented NAND logic with parallel-connected structure instead of series-connection and were able to design a NAND-gate merged F/F with minimum delay.

III. PROPOSED DUAL MODULUS PRESCALER

Fig. 4 is a block diagram of the proposed 16/17 dual modulus prescaler. All the building blocks are implemented with current mode logic (CML) circuits in order to achieve fast operation speed with minimum switching noise [3-4]. For further improvement of operation speed, all the logic gates are merged into F/F's. The F/F's used in the prescaler have CML structure as in Fig.5. The size of the transistors and the biasing conditions are chosen for minimum parasitics while achieving the required operation speed.

A. Synchronous divider

Fig. 6 is the first F/F of synchronous divider which has NAND logic merged into the input transistors. Conventionally, logic function merged F/F's have series-connected transistors as in Fig. 3, resulting in increased switching delay, but we eliminated series connection by employing the feedback of the output of NOR logic. Therefore, merged NAND D-F/F with parallel connection offers improved switching speed due to the reduced effective resistance.

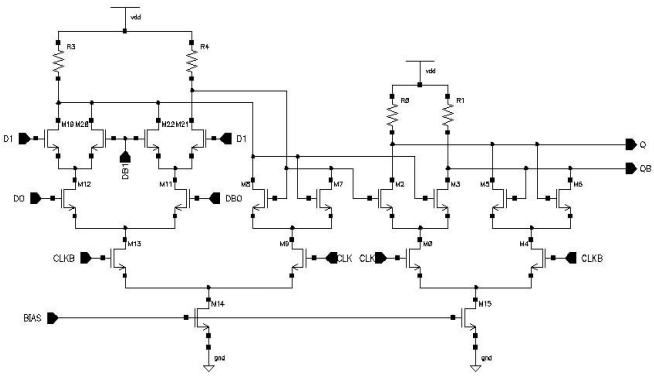


Fig. 3. Merged NAND D-F/F with series-connection

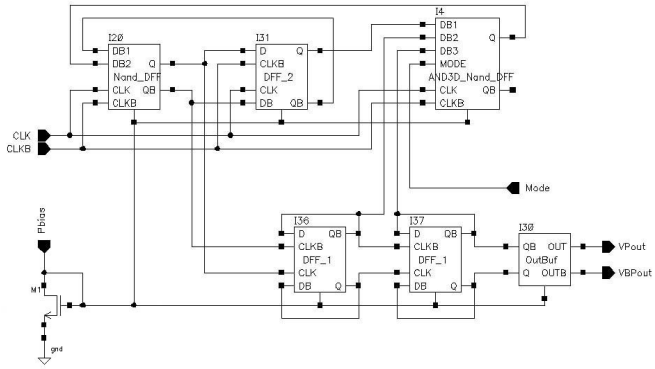


Fig. 4. Proposed high speed dual modulus prescaler

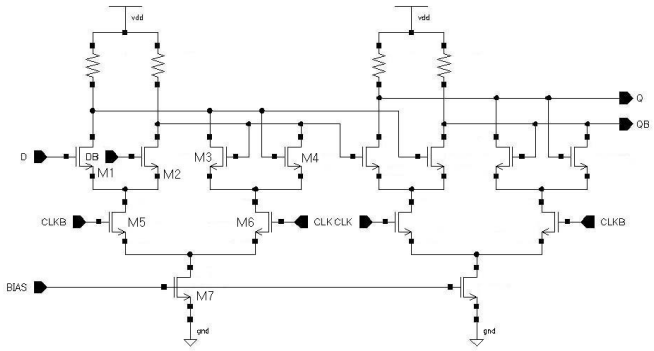


Fig. 5. Current-mode logic D-F/F

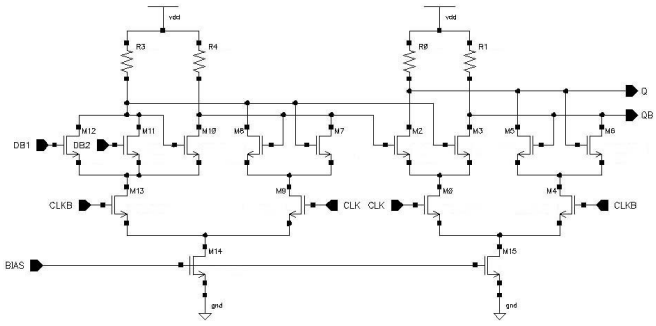


Fig. 6. Merged NAND D-F/F with parallel-connection

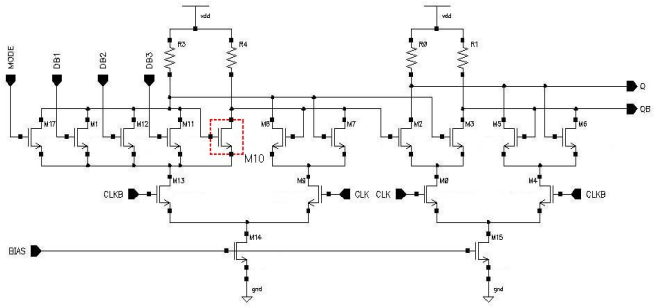


Fig. 7. Merged 3-input AND & NAND D-FF

Fig. 7 is the F/F that has two inputs from the asynchronous divider which are NAND gate with the output of the preceding F/F and MODE selection signal. For this flip-flop, it is important to get accurate swallow pulse. If the feedback transistor M10 is sized to be equal to the input transistors, the current switching cannot be done properly because of the unequal strength. Therefore, the feedback transistor is sized to be approximately two times larger than the input transistors.

B. Asynchronous divider

The divide-by-4 asynchronous divider is made of 2 cascaded divide-by-2 circuits which use the same type of CML F/F's as in synchronous divider. Of course, the F/F's of the asynchronous divider is designed draw less current than those in the synchronous divider because it is clocked at to lower frequency.

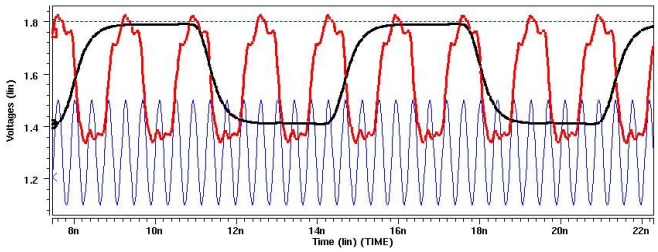
At the final output of the dual modulus prescaler, a two stage buffer is added to drive the external 50Ω load.

IV. SIMULATION RESULTS

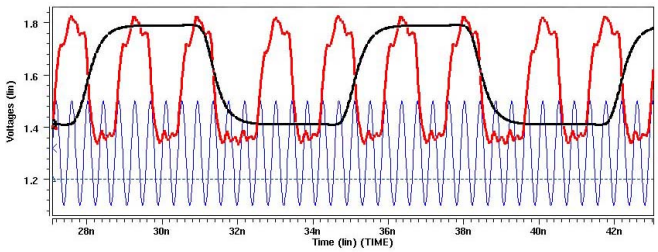
The dual modulus prescaler was simulated including the effect of all the parasitics with a standard 0.35μm CMOS technology. The simulated operating frequency range is from 0.8 to 3.1 GHz at 1.8V supply voltage. From a 1.8V power supply, the prescaler draws about 14mA current, including the buffers driving the external 50Ω load. Fig. 8 shows the output waveform of divide-by-16 and divide-by-17 outputs at 2.4GHz clock. Fig. 9 shows the operating waveforms at 3.1GHz clock when connected to 50Ω load.

V. CONCLUSIONS

A high speed dual modulus prescaler is implemented in 0.35μm CMOS process. The maximum operating frequency is 3.1GHz. Including the buffer, the circuit draws about 14mA from a 1.8-V supply. It is expected that the proposed dual modulus prescaler can be effectively used in a multi-GHz frequency synthesizer.



(a) divide-by-16 when MODE is high



(b) divide-by-17 when MODE is low

Fig. 8. Divide-by -16/17 output waveforms at 2.4GHz clock

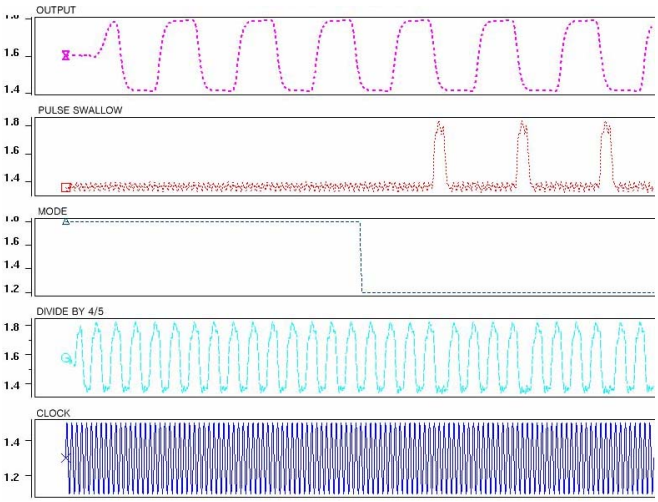


Fig. 9. 3.1GHz operation waveform

VI. ACKNOWLEDGMENT

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REFERENCES

[1] J. Craninckx and MSJ Steyaert, "A Fully Integrated CMOS DCS-1800 Frequency Synthesizer," IEEE Journal of Solid-State circuits, vol. 33, pp. 2054-2065, 1998.

[2] C. Yang, et al. "New Dynamic Flip-Flops for High-Speed Dual-modulus Prescaler," IEEE JSSC, vol. 33, no. 10, pp. 1568-1571, Oct. 1998.

[3] Ranganathan Desikachari, "High-speed CMOS Dual Modulus Prescaler Design Review", Nov. 2002. MS. Thesis. Oregon State University.

[4] Ajjikuttira.A.B and W.L.Chan. and Y.Lian, "A 5.5GHz Prescaler in 0.18-μm CMOS Technology," ASIC, 2002. Preceding. 2002 IEEE Asia-Pacific conference on 6-8 Aug. 2002. Page : 69-72