Chapter 5

Flyback Converters

The flyback converter has long been popular for low-power applications. The major attraction of the flyback topology is its low component count. At higher power levels, the output capacitor ripple current is often too great to deal with using conventional, low-cost capacitors. Dynamic response is also limited in continuous conduction mode, because of a right-half-plane (RHP) zero in the transfer function.

In the flyback topology, energy is stored in a power inductor (which often has multiple windings, as in a transformer) during the on-time of the switch. During the off-time of the switch, the energy is delivered to the load. The flyback topology is often used in both discontinuous and continuous conduction modes and can be successfully controlled using current mode or voltage converters.

A Flyback Subcircuit

A simplified functional schematic diagram of the flyback subcircuit is shown in Fig. 5.1. It is included in the Power IC Model Library for PSpice available from AEi Systems. It is a universal subcircuit that is capable of simulating the flyback regulator in both the continuous and discontinuous modes of operation with either voltage mode or current mode control. The derivation of the model is as follows.

Defined terms

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{in}$</td>
<td>Converter input power</td>
</tr>
<tr>
<td>$L_m$</td>
<td>Power transformer magnetizing</td>
</tr>
<tr>
<td>$I_{\min}$</td>
<td>Minimum primary current</td>
</tr>
<tr>
<td>$V_C$</td>
<td>Offset error amp output</td>
</tr>
<tr>
<td>$N_P$</td>
<td>Power transformer ratio</td>
</tr>
<tr>
<td>$V_{out}$</td>
<td>Subcircuit output voltage</td>
</tr>
</tbody>
</table>

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$I_{\text{max}}$  Peak primary current  $I_{\text{out}}$  Average output current

$F_{\text{sw}}$  Switching frequency  $R_b$  Current transformer burden

$\eta$  Efficiency factor  $N_C$  Current transformer ratio

$T_s$  Propagation delay  $D$  Converter duty cycle

$T_{\text{on}}$  MOSFET on-time  $P_{\text{out}}$  Converter output power

$V_{\text{in}}$  Converter input voltage

**Governing equations**

$$P_{\text{out}} = P_{\text{in}} \cdot \eta$$

$$P_{\text{in}} = \frac{1}{2} L_m \left( I_{\text{max}}^2 - I_{\text{min}}^2 \right) F_{\text{sw}}$$

$I_{\text{max}}$ is defined by the control Voltage $V_c$ as

$$I_{\text{max}} = \frac{V_c N_C}{R_b} + \frac{V_{\text{in}} T_s}{L_m}$$

The MOSFET on-time is calculated as

$$T_{\text{on}} = \frac{L_m (I_{\text{max}} - I_{\text{min}})}{V_{\text{in}}}$$

Since $T_{\text{on}} = D/F_{\text{sw}}$,

$$D = \frac{L_m F_{\text{sw}} (I_{\text{max}} - I_{\text{min}})}{V_{\text{in}} N_P - V_{\text{out}}}$$
During the MOSFET off-time, the primary current falls as
\[
I_{\text{max}} - I_{\text{min}} = \frac{V_{\text{out}} (1 - D)}{N_p L_m F_{\text{sw}}} \quad \text{while} \quad I_{\text{max}} - I_{\text{min}} \geq 0
\]
Substituting equations,
\[
I_{\text{min}} = I_{\text{max}} - \frac{V_{\text{out}}}{N_p} \left( 1 - \frac{L_m F_{\text{sw}}}{V_{\text{in}} (I_{\text{max}} - I_{\text{min}})} \right)
\]
which can be further simplified as
\[
I_{\text{min}} = I_{\text{max}} - \frac{V_{\text{out}}}{N_p L_m F_{\text{sw}} \left( 1 + \frac{V_{\text{out}}}{N_p V_{\text{in}}} \right)} \quad \text{while} \quad I_{\text{min}} \geq 0
\]
Substituting equations,
\[
I_{\text{out}} = \frac{L_m F_{\text{sw}} \left( I_{\text{max}}^2 - I_{\text{min}}^2 \right)}{2} \left( \frac{1}{V_{\text{out}}} + \frac{1}{V_{\text{in}} N_p - V_{\text{out}}} \right) \eta
\]
and the duty cycle can be calculated as
\[
D = \frac{L_m F_{\text{sw}} (I_{\text{max}} - I_{\text{min}})}{V_{\text{in}} N_p - V_{\text{out}}}
\]
The circuit shown in Fig. 5.2 is a simple representation, using the new subcircuit, of a dual-output flyback converter with a separate transformer winding for voltage regulation. The flyback subcircuit essentially replaces the PWM switch model discussed in Chap. 4.

The results of the gain-phase measurement of the flyback converter are shown in Figs. 5.3 and 5.4 for a 30-mA load and a 1-A load on each output, respectively. The circuit has a bandwidth of 7 kHz with a phase margin of 75° and a 1-A load. At a 30-mA load, the performance is quite different because of the discontinuous operation. The 34 kHz would likely be a problem for most applications. Either the converter would require a preload or the 1-A load bandwidth would have to be reduced. This would sacrifice performance.

Note that L1 and C4 are used to break the loop for the open-loop measurement. Voltage source V4 represents the injection signal. This method allows the DC path to be closed via L1, while the AC information is removed (essentially) by the very low frequency filter created by L1 and C4.

**Audio Susceptibility**

The same SPICE model can be used to evaluate closed-loop performance parameters, such as audio susceptibility. To use the model for these
Figure 5.2  Schematic design and netlist for a dual-output flyback converter.
evaluations, the inductor, capacitor, and AC voltage source can be left in the circuit. This is accomplished by changing the value of L1 to 1 pH, and C4 to 1 pF. To simulate the audio susceptibility performance, an AC source statement must also be added to the input voltage source, V1.

The results of the audio susceptibility simulation are shown in the graph of Fig. 5.5.
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Figure 5.4  Gain-phase Bode plot of the dual-output flyback converter with a 30-mA load on each output.

Figure 5.5  Audio susceptibility simulation results, node 11.
Feedforward Improvements

The flyback converter has a peak input current that varies with input voltage.

This can be seen by sweeping the input voltage and monitoring the control voltage or the output of the error amplifier (see Fig. 5.6).

Although this curve is not linear, the audio susceptibility of the flyback converter can still benefit from feedforward compensation. This is most easily added via a simple resistor connected from the input voltage to the current sense pin of the PWM IC. We can add a feedforward signal in series with the control pin of the subcircuit to accomplish the same effect.

The schematic showing the incorporation of the feedforward signal is shown in Fig. 5.7.

The improvement in audio susceptibility is graphically shown in Fig. 5.8. Note that the feedforward signal improves the audio susceptibility performance by more than 20 dB. In several applications, I have been able to use this feedforward technique, rather than adding a linear regulator, to obtain the necessary attenuation. There are several benefits. There is no reduction in efficiency performance, as would occur with the addition of a linear regulator. Also, the converter can be made smaller and less expensively without the linear regulator.
FLY2: FEEDFORWARD SIGNAL
.OPTION GMIN=10N
.NODESET V(2) = 15.7
*.TRAN 10U 4M 2m 10u
.PROBE
.AC DEC 25 100 1MEG
*ALIAS V(11)=+15
*ALIAS V(3)=SENSE
*ALIAS V(6)=FDBCK
*ALIAS V(18)=–15
*ALIAS V(5)=D
.PRINT AC V(6) VP(6)
.PRINT AC V(11) VP(11) V(3)
.PRINT TRAN V(3) V(18) V(5)
V1 1 0 28 AC 1
X3 2 0 13 4 TURNS Params: NUM=18
X4 9 0 13 4 TURNS Params: NUM=18
X5 0 7 13 4 TURNS Params: NUM=18
X6 3 0 13 4 TURNS Params: NUM=12
D1 9 11 DN5806
D2 18 7 DN5806
C1 11 0 100U
C2 0 18 100U
* I1 0 11 pulse 0 0.5 .1u .1u 1m 2m ; use for load step analysis
R1 1 11 0 15
R2 0 18 15
R3 4 0 1MEG
X7 8 21 0 6 16 14 UC1843AS
R4 3 21 8K
R5 21 0 2.5K

Figure 5.7 Feedforward signal schematic and netlist.
Flyback Transient Response

The transient response of the flyback converter is unaffected by the addition of the feedforward signal. The transient response simulation results in Fig. 5.9 show an overlay of a 0.5-A step on the +15-V output with and without the feedforward signal.

To calculate the DC output resistance, we use the following equations:

\[ \Delta I_1 = \frac{15 \times 0.64}{25 \mu (250 \text{ kHz})} = 1.536 \text{ A} \]
\[ I_{pk} = \frac{I_{out} \Delta I_1}{D} + \frac{0.833}{0.64} + \frac{1.536}{2} = 2.069 \text{ A} \]
\[ I_{rms} = \frac{I_{out}}{\sqrt{D}} = \frac{0.833}{\sqrt{0.64}} = 1.04 \text{ A} \]

Figure 5.7 (Continued).

Figure 5.8 Graph showing improvement in audio susceptibility.
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\[ I_{\text{cap}} = I_{\text{out}} \sqrt{\frac{1}{D}} + D = 0.833 \sqrt{\frac{1}{0.64} + 0.36} = 1.15 \text{ A} \]

\[ P_{\text{loss}} = \frac{1}{2} L_1^2 I_{pk}^2 F_s + I_{\text{rms}}^2 (\text{DCR}) + I_{\text{cap}}^2 (\text{ESR}) \]

\[ = \frac{1}{2} \left( 350 \text{ nH} \right) (2.07)^2 250 \text{ kHz} + (1.04)^2 0.1 + (1.15)^2 0.03 \]

\[ = 0.335 \text{ W} \]

\[ R_{\text{eff}} = \frac{P_{\text{loss}}}{I_{\text{out}}^2} + R_{d} = \frac{0.188}{(0.833)^2} + 0.12 = 0.483 + 0.12 = 0.603 \Omega \]

The resulting 0.6 \Omega is a good approximation of the DC output resistance. Based on our example, the load regulation from 10\% to 100\% load would be

\[ \Delta V = 0.833 \times 0.9 \times 0.6 = 0.45 \text{ V} \]

The actual value that was recorded for the converter was 0.49 V. Obviously, the resistance is nonlinear and dependent upon input voltage, but this is a good estimate.

The calculated output resistance was implemented into this SPICE model in order to get the simulation results of Fig. 5.11.
From the previous simulation, we can obtain the nominal duty cycle of 0.36 with an input voltage of 28 V, or we could calculate it as

\[ D = 1 - \frac{V_{\text{in}}}{V_{\text{out}}} \]

The delta inductor current can be calculated on the basis of the output voltage and \( D' \):

\[ \Delta I_1 = \frac{V_{\text{out}}D'}{L_s F_s} \]

The peak secondary current is calculated as

\[ I_{\text{pk}} = I_{\text{out}} \frac{D'}{2} + \Delta I_1 \]

The secondary RMS current can be approximated by

\[ I_{\text{rms}} = \frac{I_{\text{out}}}{\sqrt{D'}} \]

The output capacitor RMS ripple current is calculated as

\[ I_{\text{cap}} = I_{\text{out}} \frac{1}{\sqrt{D'} + D} \]

The effects of the diode forward drop can best be approximated by evaluating the difference in forward voltage at two output currents of interest as

\[ R_d = \frac{\Delta V_f}{\Delta I_{\text{out}}} \]

The parameters from the power supply design are listed in the following table.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L_1 )</td>
<td>350 ( \mu )H</td>
</tr>
<tr>
<td>( L_s )</td>
<td>25 ( \mu )H</td>
</tr>
<tr>
<td>ESR</td>
<td>0.03 ( \Omega )</td>
</tr>
<tr>
<td>( D )</td>
<td>0.36</td>
</tr>
<tr>
<td>( N )</td>
<td>1</td>
</tr>
</tbody>
</table>

Simulating Regulation

One of the more difficult simulations to perform is the DC regulation of the flyback converter. The regulation and, more importantly, the cross-regulation of a flyback converter is a function of the parasitic leakage.
inductance of the power transformer, the output rectifier characteristics, and the output capacitor equivalent series resistance (ESR).

In simple terms, these losses can be viewed as linear power losses. Although this is not entirely true, it will generally provide reasonably accurate results. The one characteristic that will not show up is the large voltage at the output under light-load or no-load conditions. This does not generally pose a problem because there is a protection or limiting device (such as a zener diode) present to make this voltage predictable.

The following example is from an actual dual-output 15-V power supply that was designed recently (see Fig. 5.10). Given the following parameters, we will calculate the regulation for incorporation into our SPICE model.

**Definitions**

$L_1$  
Power transformer secondary leakage inductance

$I_{out}$  
Output DC current

$L_s$  
Power transformer secondary inductance

$F_s$  
Switching frequency

ESR  
Output capacitor ESR

DCR  
Transformer secondary resistance

$D$  
Duty cycle

$D'$  
1 Duty cycle

$N$  
power transformer turns ratio

$I_{rms}$  
RMS secondary current
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$I_{pk}$  Peak secondary current  \( \Delta I_1 \)  Secondary inductor current delta  
\( R_d \)  Effective diode resistance  \( R_{\text{eff}} \)  Effective average resistance  
\( I_{\text{cap}} \)  Output capacitor RMS current

The total loss of the secondary can be calculated as

\[
P_{\text{loss}} = \frac{1}{2} L_1 I_{2}^2 F_s + I_{2}^{\text{rms}} DCR + I_{\text{cap}}^2 ESR
\]

FLY3: FEEDFORWARD SIGNAL  
.OPTION RELTOL=.01 ABSTOL=0.1u VNTOL=10u GMIN=10N ITL1=500 ITL4=500  
.NODESET V(2) = 15.7  
.TRAN 10U 4M 2M 1u  
.PROBE
  * V(11)=+15  
  * V(3)=SENSE  
  * V(6)=FDBCK  
  * V(18)=-15  
  * V(5)=D  
.PRINT TRAN V(3) V(18) V(5)
V1 1 0 28  
X3 2 0 13 4 TURNS Params: NUM=18  
X4 9 0 13 4 TURNS Params: NUM=18  
X5 0 7 13 4 TURNS Params: NUM=18  
X6 3 0 13 4 TURNS Params: NUM=12  
D1 10 11 DN5806  
D2 18 15 DN5806  
C1 11 0 100U  
C2 0 18 100U  
I1 0 11 pulse 0 0.5 .1u .1u .1u 1m 2m  
R1 11 0 15  
R2 0 18 15  
R3 4 0 1MEG  
X7 8 21 0 6 16 14 UC1843AS  
R4 3 21 6K  
R5 21 0 2.5K  
C3 8 12 1N  
R6 12 21 47K  
V3 16 0 15  
EB1 6 17 Value= {.005^*V(1)}  
R7 9 10 .6  
R8 7 15 .6  
X1 1 0 17 2 5 FLYBACK Params: L=20U NC=100 NP=1 F=250K EFF=1 RB=10  
+ TS=.25U  
.END

The simulation results are shown in Fig. 5.11 along with the previous transient simulation results in order to see the effect of the output resistance.
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Time Domain Model

The next simulation shows the basic configuration for a transient model of an off-line flyback converter (see Fig. 5.12). The transient model allows us to investigate details within the converter, such as peak switch current, harmonic content, output ripple voltage, and many other phenomena that would not be observable using a state space model.

Although this model is somewhat simplified, it can easily be upgraded even further. Upgrades could include a nonlinear core model for the power transformer, an input EMI filter, multiple outputs, transformer leakage inductance, etc. In most cases, it is recommended that you start with a basic power supply representation such as this and then add the required details. In fact, each piece can be simulated separately before they are all put together. Using this approach you will have more assurance that the final model will converge, and you can make any necessary changes to the subsections by taking advantage of the superior simulation speed. Obviously, as the model complexity increases, the run time will also increase, thus making investigation of the behavior of each subsection more costly.

The simulation results of the transient model are shown in Fig. 5.13.
LT1243: OFF-LINE FLYBACK CONVERTER

*SPICE.NET
.TRAN 0.1US 0.6MS .1MS 10n UIC
.PROBE
.OPTIONS RELTOL=.005 ITL4=300
* V(9)=VPRIM
* V(16)=VOUT
* V(12)=VSECOND
* V(17)=ISENSE
* V(26)=VERR
.PRINT TRAN V(9) V(16) V(12) V(17) V(28)
V3 2 0 350V
R2 16 0 15
C2 16 3 68UF IC=-14.8V
R3 1 2 2
X5 2 9 12 0 XFMR Params: RATIO=-0.05
R6 3 0 45M
D1 12 16 DIODE OFF
.MODEL DIODE D (TT=1NS CJO=1PF RS=1M)
X7 28 21 17 27 0 11 15 25 LT1243
R8 14 0 2.8
V9 15 0 PULSE 0 15 0 1U
R9 17 14 1K
C4 17 0 1NF
C5 27 0 4.7NF
R10 27 25 3K
R12 21 28 146K
C6 21 28 56P

Figure 5.12 Schematic for an off-line flyback converter using a PWM IC model capable of showing all key transient effects. The top-level netlist is also shown.
R13 21 16 50K
R14 21 0 10K
S9 9 14 11 0 SW
.MODELSW VSWITCH RON=.1 VON=5 VOFF=3 ROFF=1E6
L1 1 9 4MH IC=0
.END

Figure 5.12  (Continued)

Figure 5.13  Transient model results.
Adding Slope Compensation

The schematic in Fig. 5.14 shows the addition of an external ramp to provide slope compensation to the model. The $D$ output of the subcircuit is provided for this purpose. The $D$ output is a voltage equivalent of the duty cycle; so a ramp is defined as $K*D$, where $K$ is the peak voltage of the ramp at a duty cycle of 1. $K$ can also be described as the slope of the ramp divided by the switching frequency.

Although we do not have access to the internal nodes required to add the ramp, we can rotate it through the comparator and easily add it externally. A nonlinear dependent source is used to provide the multiplication of $K$ and $D$. The schematic in Fig. 5.15 shows the implementation of the slope compensation ramp that is external to the subcircuit.
Voltage Mode Control

Using a further extension of the circuit shown in Fig. 5.15, voltage mode control (also called duty cycle control) can be implemented. In this case there is no current sensed, so RB would ideally be set to zero. However, RB cannot be set to zero because it would result in a “divide by zero error” within the subcircuit. It can, however, be set to a very low value such as 1 mΩ or lower, if necessary. Setting $K$ to 1 will result in a duty cycle that is equal to the control voltage, $V_C$. The modulator gain may also be represented in this subcircuit by setting $K$ equal to $1/V_r$, where $V_r$ is the peak-to-peak voltage of the ramp. Within the subcircuit, $V_C$ is bounded between 0 and 1 V. To use this limiting function, it is recommended that you set $K$ to 1 and add the modulator gain externally.