Efficiency Comparison between Doubler and Dickson Charge Pumps

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***Abstract*— This paper presents a comparison between two of the most popular charge pump structures: the Dickson charge pump and the cascade of voltage doublers. The comparison has been carried out considering the power efficiency as the main parameter of interest. The discussion is supported by theoretical analysis and experimental results. To compare the two topologies, two voltage elevators were designed and integrated in a triple-well 0.18-μm CMOS technology. The two charge pumps were designed with the same operating clock frequency, the same storage capacitance per stage, and the same number of stages (and, thus, approximately the same area). The comparison showed that the voltage doubler has a power efficiency higher by about 13%.**

I. Introduction

The scaling down of transistor channel length and oxide thickness leads to a continuous reduction of supply voltages in integrated circuits. Nevertheless, several devices (such as LCD displays, non volatile memories, and smart power devices) require operating voltages higher than the power supply. In these devices, it is therefore mandatory to integrate DC-DC voltage converters (which are referred to as voltage elevators), so as to generate the required high voltages from the available supply voltage V_{DD}. Fig. 1 shows a schematic diagram of DC-DC voltage converter.

The most popular schemes for voltage elevator are based on the charge pump approach [1]. Charge pumps are commonly used to generate both positive and negative high voltages. In the case of portable applications, a key issue is to minimize power consumption. One of the most important figures of merit of voltage elevator topologies is therefore power efficiency, hereinafter referred as efficiency for simplicity.

The efficiency η of a voltage elevator is defined as the ratio between the power P_{out} delivered to the load and the power P_{in} drawn from the supply V_{DD}. The input power P_{in} is equal to the sum of the output power P_{out} and the overall power losses P_{loss} and, hence, the value of η can be expressed as:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}}. \quad (1)$$

In this paper, we present the theoretical and the experimental comparison between two of the most popular schemes for integrated charge pumps (i.e., the Dickson and the voltage doubler topologies). Section II gives a basic description of the Dickson charge pump and the voltage doubler. A theoretical analysis is presented in Section III, whereas in Section IV efficiency comparison is carried out. Experimental results which confirm the theoretical analysis are shown in Section V.

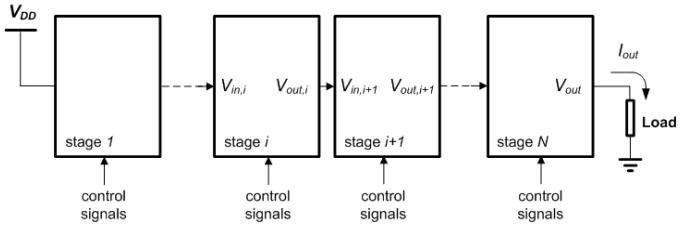

Fig. 1. Schematic representation of a generic DC-DC voltage converter. Control signals are required to properly drive the voltage elevator.

II. Dickson and Doubler Structures

The Dickson charge pump [1], [2] is widely used in Flash memory chips for high-voltage generation. Two cascaded stages of an integrated CMOS Dickson scheme are shown in Fig. 2. Since the voltage increase provided by a single stage is (ideally) equal to V_{DD}, a complete Dickson charge pump is typically obtained as the cascade of a suitable number N of identical stages, which ideally gives an output voltage equal to $(N+1) \cdot V_{DD}$.

In order to generate the required high voltage, the charge stored in each capacitor $C_{DK,i}$ is transferred to the capacitor $C_{DK,i+1}$ of the next stage through a switch, M_{i+1}. To prevent undesired voltage drop across switches M_{i+1}, boosting circuits must be used so as to reduce the switch on-resistance. To this end, additional switches (M_i') and capacitors ($C_{BST,i}$) are needed. Due to the presence of the boosting elements, the structure requires four non-overlapping control signals: ϕ_1 and ϕ_3 are used to charge the pump capacitors ($C_{DK,i}$), whereas ϕ_2 and ϕ_4 are used to boost the gates of switches M_i' during charge transfer.

During the charge transfer from $C_{DK,i}$ to $C_{DK,i+1}$ a voltage drop of about twice the supply voltage V_{DD} is applied across the gate oxide of M_i'. To prevent excessive electrical stress, high-voltage transistors must therefore be used. The main disadvantage of these devices is their high threshold voltage, which calls for a large gate area and, as a consequence, leads to a large parasitic capacitance (as compared to

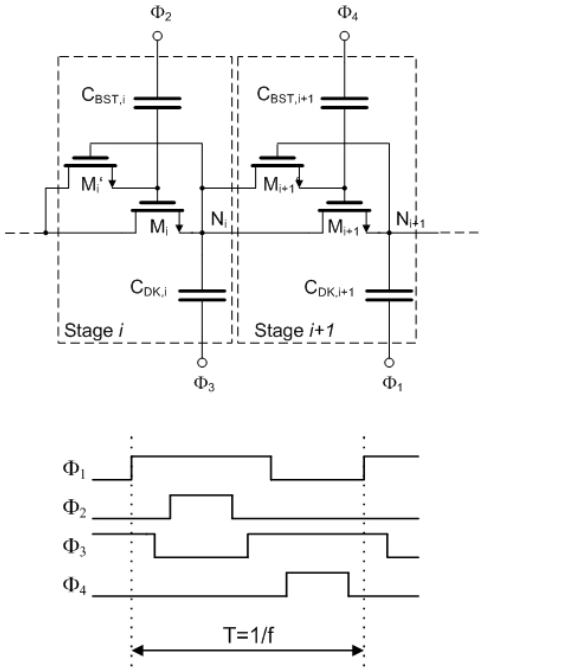

Fig. 2. Two cascaded stages of a Dickson charge pump.

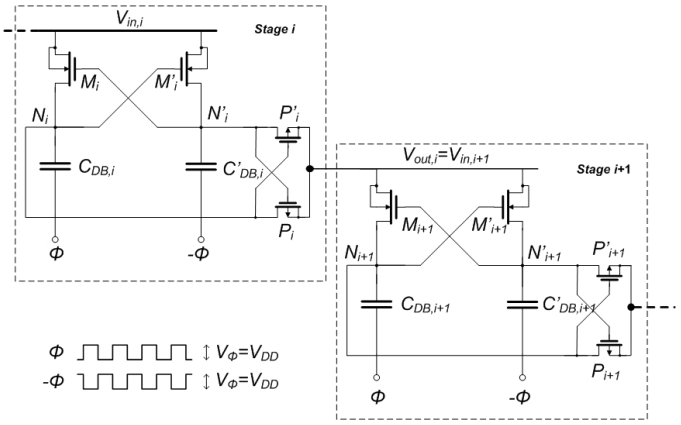

Fig. 3. Two stages of a cascade of voltage doublers.

the parasitic capacitance of low-voltage switches). In practice, this large parasitic capacitance reduces the maximum allowed frequency, f_{max}, of the control phases. Therefore, for any value of the required output resistance (which is given by $R_{out} = N/(f \cdot C_{DK})$), a limit on the maximum operating frequency results in the need for larger storage capacitors, thus leading to larger silicon area occupation.

On the other hand, Fig. 3 shows the structure of two cascaded stages of a voltage doubler [3], [5]. The main advantage of this structure, as compared to a Dickson charge pump, is represented by a simpler clock distribution since a two phase clock scheme is required. As a further advantage, this structure does not require the use of additional boosting elements. In practice, a stage of a voltage doubler consists of a pair of storage capacitors, $C_{DB,i}$ and $C'_{DB,i}$, a pair of cross-connected NMOS switches, M_i and M'_i, used to charge the capacitors, and a pair of PMOS transistors, P_i and P'_i, used as transfer elements. Also in this case, more stages are cascaded (i.e., $V_{out,i}$ is connected to $V_{in,i+1}$), to obtain an output voltage larger than $2V_{DD}$. During charge transfer from the storage element $C_{DB,i}$ of the i-th stage to the storage element $C'_{DB,i+1}$ of the $(i+1)$-th stage, P_i and M'_{i+1} are activated. It is worth to point out that the voltage drop across any device is never larger than V_{DD}. This means that standard low-voltage MOS transistors can be used. As mentioned above, this structure does not require additional boosting elements. In fact, during the operating phase ϕ ($-\phi$), the upper plate of $C_{DB,i}$ ($C'_{DB,i}$), and hence, the gate of M'_i (M_i) are boosted, thus reducing the on-resistance of the pre-charge transistor M'_i (M_i).

III. Power Efficiency Analysis

To calculate the efficiency η of a voltage elevator, the overall power losses P_{loss} must be evaluated. Since a voltage elevator is basically a switched-capacitor network, this term includes the contribution of both the resistive losses P_{res} and the dynamic losses P_{dyn} (where the short circuit power consumption of the clock phase drivers is neglected since they are assumed to be much lower than P_{dyn}). In general, an N-stage Dickson or doubler charge pump can be modeled as an ideal voltage source with an open-circuit output voltage approximately equal to $(N+1)V_{DD}$ and an ideal series output resistance $R_{out,id} = N/fC$ (where C is equal to C_{DK} and $2C_{DB}$, for the Dickson and the doubler scheme, respectively). With these assumptions, the resistive power losses P_{res} are given by $R_{out,id}I^2_{out}$, while the dynamic power losses P_{dyn} can be considered to be proportional to $NfC_{par}V^2_{DD}$ (where C_{par} is the equivalent parasitic capacitance in each stage). By using the above relations, it is possible to represent the power efficiency η as [4]:

$$\eta = \frac{V_{out}I_{out}}{V_{out}I_{out} + P_{res} + P_{dyn}} = \tag{2}$$

$$= \frac{V_{out}I_{out}}{V_{out}I_{out} + R_{out,id}I^2_{out} + kNfC_{par}V^2_{DD}}$$

where k is a suitable coefficient of proportionality which depends on the topology of the voltage elevator, V_{out} and I_{out} are the mean values (over a clock period) of the output voltage and the output current, respectively. The product $V_{out} \cdot I_{out}$ is the mean power (P_{out}) delivered by the pump to the load.

In the case of Dickson and doubler charge pumps [1], when the parasitic elements are taken into account, the output voltage can be expressed as:

$$V_{out} = \frac{C}{C + C_{top}} \cdot [(N + 1 + \beta) \cdot V_{DD} - R_{out,id}I_{out}] \tag{3}$$

and the effective output resistance as:

$$R_{out} = \frac{C}{C + C_{top}} \cdot R_{out,id} \tag{4}$$

where C_{top} represents the parasitic capacitance associated to the top plate of each stage capacitors. Actually, the overall parasitic capacitance per stage, C_{par}, is originated by two contributions: C_{top}, associated to the top plate of the capacitor, and C_{bott} associated to the bottom-plate. To be more specific, C_{top} and C_{bott} can be seen as a fraction of the storage capacitor C: $C_{top} = \beta C$, $C_{bott} = \alpha C$. Obviously, C_{top} and C_{bott} include all parasitic contributions (i.e., the parasitic capacitance of the storage capacitor, the interconnect lines, and the switches), and their values depend on both the pump topology and the kind of capacitor. By using (3), it is possible to calculate the maximum output current (i.e., when V_{out}=V_{DD}), $I_{out,max}$, that a charge pump can deliver to the load:

$$I_{out,max} = \frac{N \cdot V_{DD}}{R_{out,id}} = fCV_{DD}. \quad (5)$$

It is important to note that $I_{out,max}$ does not depend on the amount of the parasitic elements. This means that charge pumps with different topology heaving the same value of N, f, and C hexibit the same driving capability. Nevertheless, coefficients α and β determine the maximum efficiency value once N, f, and C are chosen. The higher α and β, the lower the maximum value of η. In the case of Dickson and doubler charge pumps, since each node of the structure has a voltage swing of about V_{DD}, the factor k can be assumed approximately equal to 1. This way, the dynamic power losses can be expressed as:

$$P_{dyn} = NfC_{par}V_{DD}^2 = (\alpha + \beta) \cdot NfCV_{DD}^2 \quad (6)$$

and the efficiency turns out to be:

$$\eta = \frac{V_{DD}I_{out}(N + 1 + \beta) - R_{out,id}I_{out}^2}{V_{DD}I_{out}(N + 1 + \beta) + (\alpha + \beta)(1 + \beta)NfCV_{DD}^2} \quad (7)$$

Typically, α depends on the kind of the storage capacitor, the phase driver and, in Dickson charge pump, the bottom plate parasitic capacitance of the boost capacitors. In particular, since the boost capacitor is much smaller than the storage capacitor, α can be assumed to be approximately independent from the pump topology. On the other hand, β strongly depends on the structure of the voltage elevator. To reduce dynamic power losses, it is mandatory to design a pump architecture that minimize the top-plate parasitic capacitances. As it will be shown in the next section, the cascaded of voltage doublers allow the power efficiency to be improved (with respect to a Dickson structure) since the dimensioning of switches can be carried out in such a way that the top-plate parasitic elements can be minimized.

IV. Efficiency Comparison

To compare the efficiency performance of the two above charge pump architectures, we must consider two charge pumps integrated with the same fabrication process (in our case, a 0.18-μm CMOS technology) and having approximately the same area, the same number of stages N, and the same output resistance R_{out}. This means that the two charge pumps must operate at the same clock frequency f, use the same value of storage capacitance C per stage and the same kind of capacitor (in our case, NMOS capacitors). The value of α for these capacitors is about 0.091. Furthermore, the switches interconnecting two cascaded stages must be designed in such a way that their on-resistance (R_{ON}) is the same in the two pumps. This way, the amount of charge transferred during one clock period is equal in the two structures.

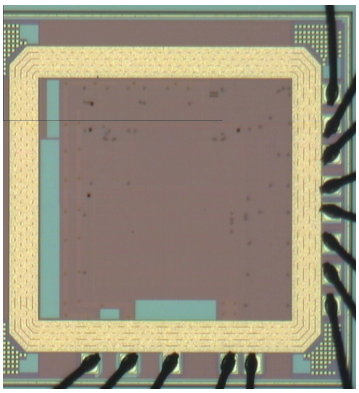

Fig. 4. Test chip micrograph.

The total top-plate stray capacitance C_{top} for a generic node N_i in Fig. 2 and Fig. 3 is given by the sum of the parasitic capacitances of the NMOS capacitor and the MOS switches. The last term is responsible for the difference between the two charge pumps. In fact, for the Dickson charge pump, this term is given by the contribution of four elements, i.e. the gate capacitance of the pre-charge transistor M_i', the drain-to-bulk capacitance of the pre-charge transistor M_{i+1}', the drain-to-bulk capacitance of pass-transistor M_{i+1}, and the source-to-bulk capacitance of the pass transistor M_i. In our case, the considered contribution to the top-plate stray capacitance $C_{top,DK}$ for the Dickson structure was calculated to be approximately equal to $0.11 \cdot C$. On the other hand, the contribution of the MOS switches to the top-plate parasitic capacitance at any node N_i in the voltage doubler topology is also given by four terms, i.e., the gate capacitance of M_i', the source-to-bulk capacitance of pre-charge device M_i, the gate capacitance and the source-to-bulk capacitance of a PMOS pass transistor (P_i' and P_i, respectively). The calculated contribution to the stray capacitance $C_{top,DB}$ for the voltage doubler is about $0.039 \cdot C$. The difference in the contribution $C_{top,DK}$ and $C_{top,DB}$ leads to a different DC-DC voltage increment per stage in the two topologies. In fact, when $I_{out} = 0$, the voltage increment per stage ΔV_{stage} is given by [1]:

$$\Delta V_{stage} = \left(\frac{C}{C + C_{top}}\right) \cdot V_{DD} \quad (8)$$

From (3), this undesired loss on the voltage increment per stage leads to a decreased output voltage of the pump and, hence, reduces the efficiency of the structure. In particular, since the Dickson scheme has a larger stray capacitance (as a consequence of the use of high-voltage transistors and the need for boosting elements), a lower output volt-

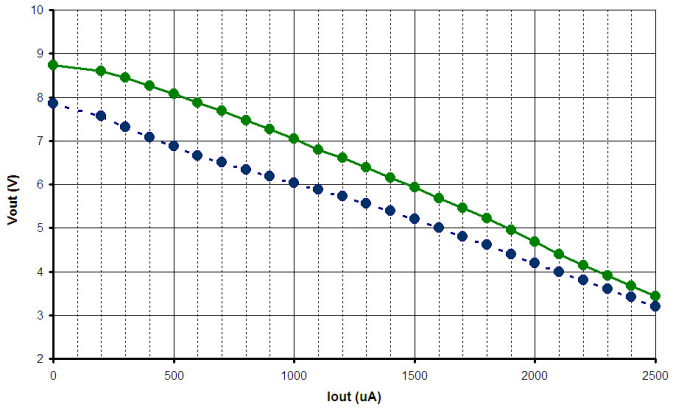

Fig. 5. Output characteristics of the voltage doubler (solid line) and the Dickson charge pump (dashed line).

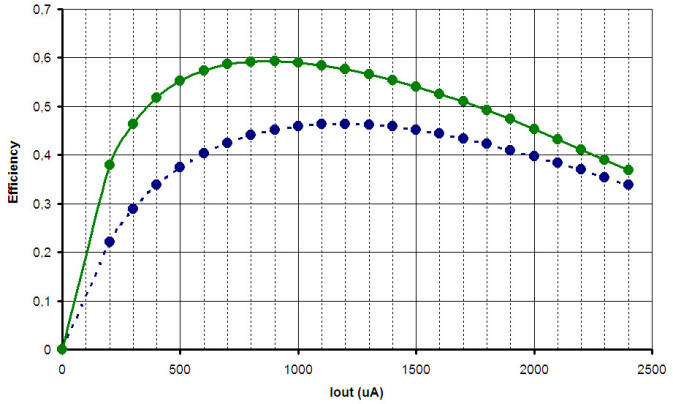

Fig. 6. Efficiency of the voltage doubler (solid line) and the Dickson charge pump (dashed line).

age and, consequently, a lower efficiency is expected for this topology with respect to the doubler scheme. A further efficiency reduction for Dickson topology derives from the presence of the bottom-plate parasitic capacitance of the boost capacitors $C_{BST,i}$ (in our case, their contribution is about $0.026 \cdot C_{DK}$). Considering the case of an N-stage charge pump with a capacitance per stage equal to 88 pF, using equations (7) and substituting the values of the parasitic capacitances ($\alpha = 0.091 + 0.026 = 0.117$ for Dickson pump and $\alpha = 0.091$ for the doubler pump), it is possible to evaluate the performance of both structures. In the case of Dickson charge pump, a maximum efficiency of 44.8% at a current of about 1 mA was calculated. On the other hand, the voltage doubler has a theoretical maximum efficiency of 56% at the same value of output current.

V. Experimental Results

To validate the above considerations, a 4-stage Dickson and a 4-stage doubler charge pump were designed, fabricated, and measured. Both pumps were integrated in 0.18-μm triple-well CMOS technology. The supply voltage and the clock frequency were set to 1.8 V and 20 MHz, respectively, for both pumps. The total storage capacitance per stage was about 88 pF (two 44-pF capacitors were used for the voltage doubler). All measurements were carried out with an external load capacitor of about 1 nF. Fig. 4 shows a micrograph of the test chip.

The measured output characteristics of the two pumps are shown in Fig. 5. The calculated output resistance R_{out} is about 2.04 kΩ for Dickson charge pump, and 2.19 kΩ for the cascade of doublers, whereas the measured output resistance was 1.87 kΩ and 2.14 kΩ for Dickson pump and the cascade of voltage doublers, respectively. Experimental results show that the Dickson pump gives an open-circuit output voltage of 7.85 V, as compared to an output voltage of 8.73 V provided by the doubler pump. The measured output voltage difference, which depends on the different values of the stray capacitances, C_{top}, is in good agreement with the value (887 mV) obtained using (8).

The measured efficiency as a function of the output current is shown in Fig. 6 for both pumps. As explained above, since dynamic losses of the voltage doubler are smaller than those of Dickson pump, the former shows higher efficiency for any value of I_{out}. From Fig. 6, the cascade of voltage doublers shows a maximum efficiency of about 59.4% at $I_{out} = 900$ μA, while the maximum efficiency of Dickson pump is 46.4% for $I_{out} = 1.2$ mA. The above values are in good agreement with the value calculated in Section IV. The measured maximum output current, $I_{out,max}$, was about 3.5 mA.

VI. Conclusion

In this work, a theoretical and experimental comparison between two of the most popular charge pump structures (i.e., the Dickson and the doubler schemes) was presented. The analytical description showed that the voltage doubler has a power efficiency higher than the Dickson charge pump (by about 13%). Experimental results are in excellent agreement with the analytical description.

Acknowledgment

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