PHASE-LOCKED LOOP SIMULATIONS USING T-SPICE

Contents:

Introduction to SPICE

Electronic circuit design requires accurate methods for evaluating circuit performance. Because of the enormous complexity of modern integrated circuits, computer aided circuit analysis is essential and can provide information about circuit performance that is almost impossible to obtain with laboratory prototype measurements. Computer aided analysis permits :

1. Evaluating the effects of variations in elements, such as resistors, transistors, transformers, and so on.
2. The assessment of performance improvements or degradations.
3. Evaluating the effects of noise and signal distortions without the need of expensive measuring instruments.
4. Sensitivity analysis to determine the permissible bounds due to tolerances on each and every element value or parameter of active elements.
5. Fourier analysis without expensive wave analyzers.
6. Evaluating the effects of non linear elements on the circuit performance.
7. Optimizing the design of electronic circuits in terms of circuit parameters.

SPICE is a general purpose circuit program that simulates electronic circuits. SPICE can perform various analyses of electronic circuits: the operating (or the quiescent) points of transistors, a time-domain response, a small-signal frequency response, and so on. SPICE contains models for common circuit elements, active as well as passive, and it is capable of simulating most electronic circuits. It is a versatile program and is widely used both in industries and universities. The acronym SPICE stands for *Simulation Program with Integrated Circuit Emphasis*.

Brief Study Of TSpice Circuit Simulations

T-Spice is designed to solve a wide variety of circuit problems. Its flexibility is due to robust algorithms which can be optimized by means of user-adjustable parameters.

Kirchoff's Current Law

T-Spice uses Kirchoff's Current Law (KCL) to solve circuit problems. To T-Spice, a *circuit* is a set of *devices* attached to *nodes*. The circuit's state is represented by the voltages at all the nodes. T-Spice solves for a set of node voltages that satisfies KCL (implying that the sum of the currents flowing into each node is zero).
In order to evaluate whether a set of node voltages is a solution, T-Spice computes and sums all the currents flowing out of each device into the nodes connected to it (its *terminals*). The relationship between the voltages at a device's terminals and the currents through the terminals is determined by the *device model.*

TYPES OF ANALYSIS

DC Analysis

The dc analysis portion of TSpice determines the dc operating point of the circuit with inductors shorted and capacitors opened. The dc analysis options are specified on the .DC, .TF, and .OP control lines. A dc analysis is automatically performed prior to a transient analysis to determine the transient initial conditions, and prior to an ac small-signal analysis to determine the linearized, small-signal models for nonlinear devices. If requested, the dc small-signal value of a transfer function, input resistance, and output resistance is also computed as a part of the dc solution. The dc analysis can also be used to generate dc transfer curves: a specified independent voltage or current source is stepped over a user-specified range and the dc output variables are stored for each sequential source value.

AC Small-Signal Analysis

The ac small-signal portion of TSpice computes the ac output variables as a function of frequency. The program first computes the dc operating point of the circuit and determines linearized, small-signal models for all of the nonlinear devices in the circuit. The resultant linear circuit is then analyzed over a user-specified range of frequencies. The desired output of an ac small- signal analysis is usually a transfer function.

Transient Analysis

The transient analysis portion of TSpice computes the transient output variables as a function of time over a user-specified time interval. The initial conditions are automatically determined by a dc analysis. All sources which are not time dependent (for example, power supplies) are set to their dc value. The transient time interval is specified on a .TRAN control line.

CIRCUIT DESCRIPTION:

GENERAL STRUCTURE AND CONVENTIONS

The circuit to be analyzed is described to TSpice by a set of element lines, which define the circuit topology and element values, and a set of control lines, which define the model parameters and the run controls. The first line in the input file must be the title, and the last line must be ".END". The order of the remaining lines is arbitrary (except, of course, that continuation lines must immediately follow the line being continued).

Each element in the circuit is specified by an element line that contains the element name, the circuit nodes to which the element is connected, and the values of the parameters that determine the electrical characteristics of the element. The first letter of the element name specifies the element type

Title Line

The title line must be the first in the input file. Its contents are printed verbatim as the heading for each section of output.

.End line

General Format:

```
.END
```

The "End" line must always be the last in the input file. Note that the period is an integral part of the name.

Comments

General Format:

```
* &ltany; comment>
```

The asterisk in the first column indicates that this line is a comment line. Comment lines may be placed anywhere in the circuit description.

DEVICE MODELS

BJT

The bipolar junction transistor model uses a modified version of the Gummel-Poon charge-control model that was implemented in the original SPICE. The model simplifies to the Ebers-Moll model when certain parameters are not specified. It also includes high-bias and temperature effects.

Parameters

The BJT model uses the following syntax.

.model name **npn**|**pnp** [parameters]

The following tables describe all of the BJT parameters that T-Spice supports. Parameters that are not specified in the Ebers-Moll model are marked with an asterisk (*).

DC Current Parameters

Parameter (alias)	*Symbol*	*Description*	*Default*	*Units*
level		Model selector	1.0	—
subs		Substrate connection selector	1 for npn; -1 for pnp	—
bf	β_f	Ideal forward maximum current gain.	100.0	—
br	β_r	Ideal reverse maximum current gain.	1.0	—
ibc	I_{bc}	Reverse saturation current between base and collector.	0.0	A
ibe	I_{be}	Reverse saturation current between base and emitter.	0.0	A
iss	I_{ss}	Reverse saturation current between bulk and collector for vertical geometry , or between bulk and base for lateral geometry	0.0	A
is	I_s	Transport saturation current.	1.0×10^{-16}	A
ise	I_{se}	Base-emitter leakage saturation current.*	**c2×is**	A
isc	I_{sc}	Base-collector leakage saturation current.*	**c4×is**	A

Parasitic Resistor Parameters

Parameter (alias)	*Symbol*	*Description*	*Default*	*Units*
irb (jrb,iob)	I_{rb}	Base current, where base resistance falls halfway between r_b and r_{bm}.*	∞	A
rb	r_b	Base resistance.*	0	Ω
rbm	r_{bm}	Minimum high current base resistance.*	rb	Ω
re	r_e	Emitter resistance.	0	Ω
rc	r_c	Collector resistance.	0	Ω

Transit time parameters

Parameter (alias)	*Symbol*	*Description*	*Default*	*Units*
ptf	P_{tf}	Frequency multiplier to determine excess phase.	0.0	deg.
tf	τ_f	Base forward transit time.	0.0	s
tr	τ_r	Base reverse transit time.	0.0	s
vtf	V_{tf}	Voltage for V_{bc} dependence of τ_f	∞	V

DIODE

The diode model has three levels.

1. Level 1 describes the Non-Geometric Junction diode model. It is used to model discrete diode devices such as standard and Zener diodes.
2. Level 2 describes the Fowler-Nordheim model that is generally used to characterize the tunneling current flow through thin insulator in nonvolatile memory devices.
3. Level 3 describes the Geometric Junction diode model. It is used to model IC-based standard silicone-diffused diodes, Schottky barrier diodes and Zener diodes.

General Format

.model name **d** [parameters]

An Abbreviated History of PLLs:

• Coincides with invention of “coherent communication” (DeBellescize, 1932).

• The earliest widespread use of PLLs was in the horizontal and vertical sweeps used in television, where a continuous clocking signal had to be synchronized with a periodic synch pulse (Wendt & Fredendall, 1943). PLLs were critical to development of color television (Richman, 1954).

• The first PLL IC arrived around 1965. This created an explosion in the use of PLLs.

• The first digital PLL appeared around 1970. This was of the classical digital PLL type.

• A few years later, the first all digital PLL appeared.

• The first laser appeared in 1960. The first optical PLL arrived 4 years later.

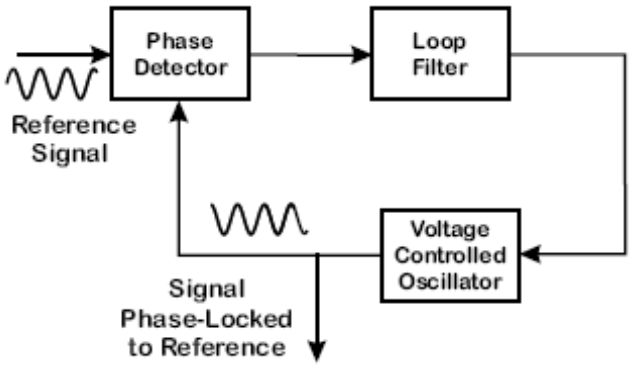
• PLLs today:

– PLLs are used in every cell phone, television, radio, pager, computer, all telephony etc.
– It is the most prolific feedback system built by engineers.
– At low end: All software PLLs implement entire PLL functionality on sampled data.
– At high end: Optical PLLs are used in clock recovery for 160 Gbps data (OFC 2002).

Introduction:

The phase-locked loop (PLL) block is a feedback control system that automatically adjusts the phase of a locally generated signal to match the phase of an input signal. PLLs operate by producing an oscillator frequency to match the frequency of an input signal. In this locked condition, any slight change in the input signal first appears as a change in phase between the input signal and the oscillator frequency. This phase shift then acts as an error signal to change the frequency of the local PLL oscillator to match the input signal. The locking-onto-a-phase relationship between the input signal and the local oscillator accounts for the name phase-locked loop.

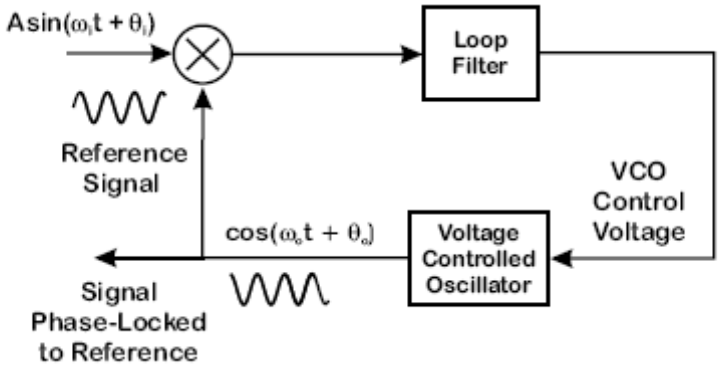
Definition:
A phase-locked loop (PLL) is an electronic circuit with a voltage- or current-driven oscillator that is constantly adjusted to match in phase (and thus lock on) the frequency of an input signal..



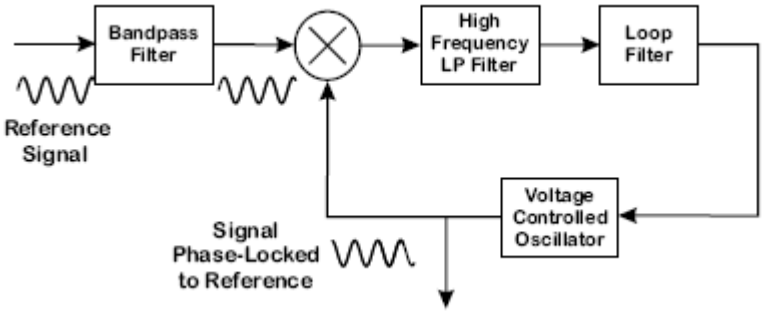
Basic idea of a phase-locked loop:

– inject sinusoidal signal into the reference input
– the internal oscillator locks to the reference input.
– frequency and phase differences between the reference and internal sinusoid =? *k* or 0
– Internal sinusoid then represents a filtered version of the reference sinusoid.
– For digital signals, Walsh functions replace sinusoids.

• A Phase Detector (PD): This is a nonlinear device whose output contains the phase difference between the two oscillating input signals.
• A voltage controlled oscillator (VCO): This is another nonlinear device which produces oscillations whose frequency is controlled by a lower frequency input voltage.
• A loop filter (LF): While this can be omitted, resulting in what is known as a first order PLL, it is always conceptually there since PLLs depend on some sort of low pass filtering in order to function properly.
• A feedback interconnection: Namely the phase detector takes as its input the reference signal and the output of the VCO. The output of the phase detector, the phase error, is used as the control voltage for the VCO. The phase error may or may not be filtered.



• General sinusoid at reference input can be written as:
Vi = R1(t) = Asin(? it + ?i).--- (1)
•Assume VCO output signal is
Vo =VCOout(t) = cos(? ot + ?o).---- (2)
• Mixer output:
Vd = Mixerout(t) = AKm sin(? it + ?i) cos(? ot + ?o),---- (3)
Where, Km is the gain of the mixer.



• Using the familiar trigonometric identity in terms of the PLL:
2sin(? it + ?i) cos(? ot + ?o) = sin((? i + ? o)t + ?i + ?o) + sin((? i - ? o)t + ?i - ?o) (4)
• Two fundamental assumptions lead to common analog PLL model.
Let ?d = ?i- ?o. Then these assumptions are:

1) The first term in (4) is attenuated by the high frequency low pass filter in and by the low pass nature of the PLL itself.
2) Let ? i ˜ ? o, so that the difference can be incorporated into ?d. This means that the VCO can be modeled as an integrator.
3) The baseband phase detector output is then:

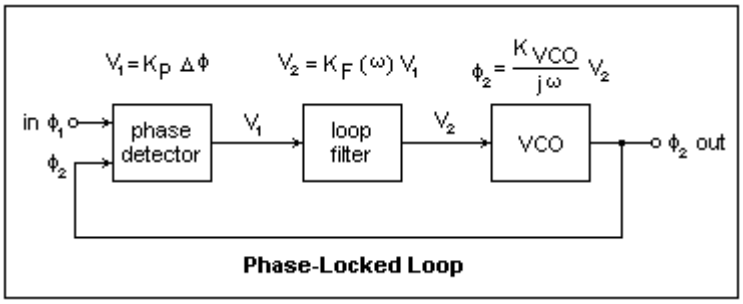
$$Vd(t) \approx \frac{AKm}{2} \sin(?i(t) - ?o(t)) = \frac{AKm}{2} \sin(?d(t))$$

How a Phase-Locked Loop Works

The phase-locked loop (PLL) is a device with many interesting applications, including frequency synthesis, FM demodulation and television sweep circuits. Its operation seems nearly miraculous, but feedback makes the job easy and it is an excellent example of feedback in action.

We will consider the fundamental phase-locked loop here. Once its operation is understood, all the applications will follow easily. We generally think of the circuit as accepting an input at some frequency and providing an output at the same frequency that is not a copy of the input, but the output of an independent oscillator whose frequency is controlled by feedback. The output of the oscillator is compared to the input and if the frequencies are different, the frequency of the oscillator is altered to reduce the difference.

This is what it looks like, but it is better to consider the controlled quantity to be the *phase* of the signals. A signal of frequency f Hz changes phase by 2pf radians per second. The phase-locked loop compares the phases of the input signal and the oscillator signal and adjusts the oscillator to reduce the phase difference. A signal flow diagram of a phase-locked loop is shown below.



The left-hand block is the *phase detector*, which compares the phases of its two input waves and provides an output V_1 proportional to the phase difference ? f . K_P is a constant with the units volts per radian. The output of the phase detector is usually in the form of pulses that have to be low-pass filtered by the *loop filter*, the middle block. This signal is then applied to the *voltage-controlled oscillator* or VCO, the block on the right. The polarities must be arranged so that if f_2 lags f_1, the VCO increases frequency slightly; that is, the feedback must be negative. The output of the VCO is fed back to the phase detector, and the feedback loop is closed.

Lock Range is the maximum frequency excursions over which the output remains locked with the input.
Capture Range is the maximum difference between the input signals frequency and oscillator's free running frequency where lock can eventually be attained.

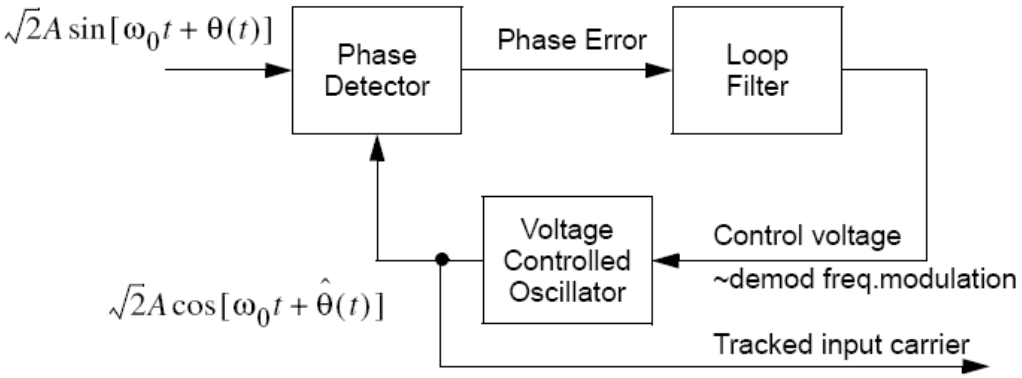
Types Of PLLs

• Analog or Linear PLL (LPLL)
• Digital PLL (DPLL)
• All digital PLL (ADPLL)
• Software PLL (SPLL)

LPLL

The LPLL (Best) or analog PLL is the classical form of PLL. All components in the LPLL operate in the continuous-time domain. A LPLL block diagram is shown below:

• The phase detector is typically some form of analog multiplier.
• The phase error function is of the form
f (t) = KmK1Asin [?(t) - ?^(t)] ˜ KD[?(t) - ?^(t)]



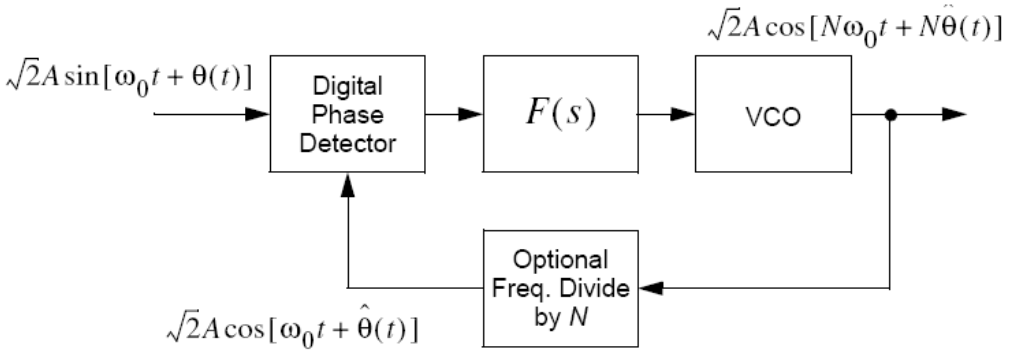
Classical analog PLL

The loop filter may be active or passive, but it typically results in the loop being either first-order or second-order.
• The design/analysis of the loop filter makes use of the Laplace transform.

DPLL

The digital PLL is really just an analog PLL with a digital phase detector.
• The DPLL is a hybrid system
• The DPLL is very popular in synthesizer applications
• In the below figure the optional digital divider, and variations on it, are used in frequency synthesis applications.

• Popular types of digital phase detectors include:
– Exclusive or gate (EXOR)
– Edge-triggered JK-flip flop
– Phase frequency detector (PFD)



Classical digital PLL (digital phase detector)

ADPLL

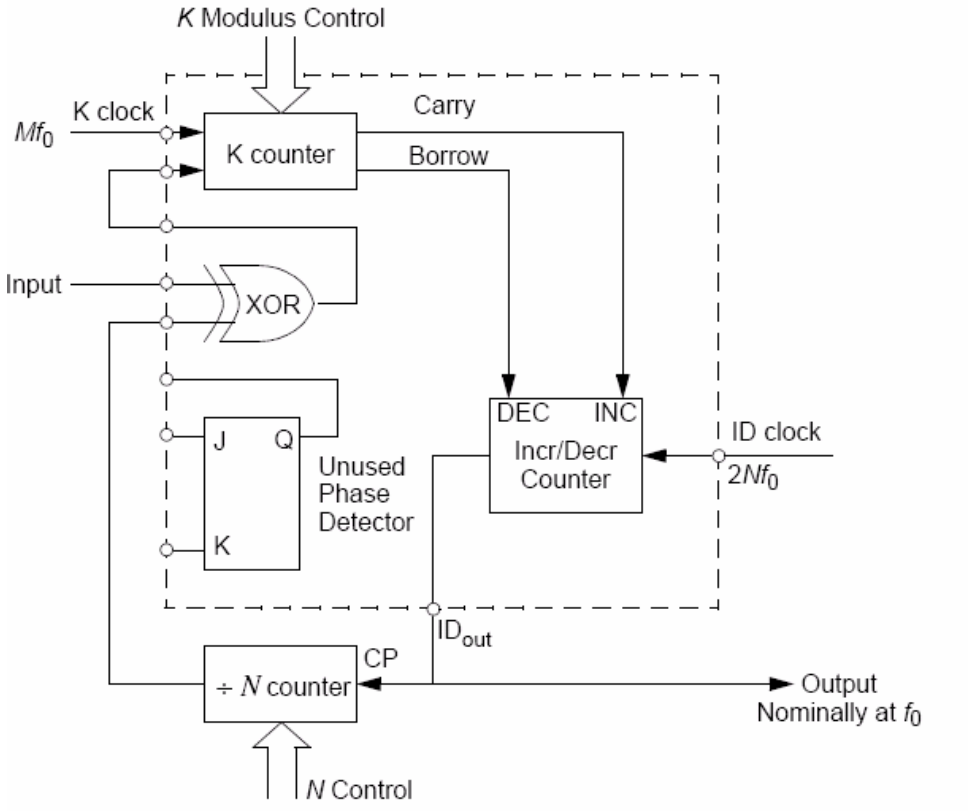
The all-digital PLL (classical all-digital) is distinctly different from the first two PLLs mentioned thus far.

• The ADPLL is a digital loop in two senses:

– All digital components

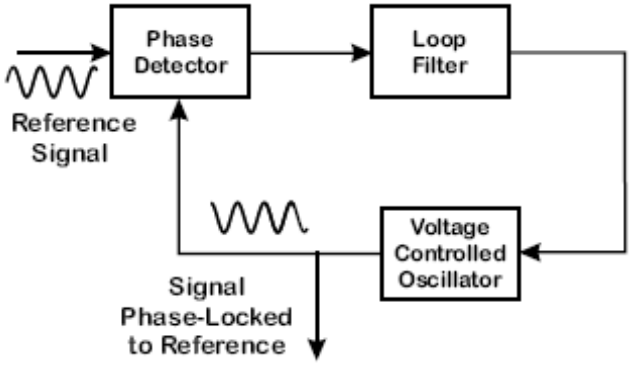
– All digital (discrete-time) signals

• The VCO is replaced by a Digitally Controlled Oscillator (DCO) or also called a Numerically Controlled Oscillator (NCO)

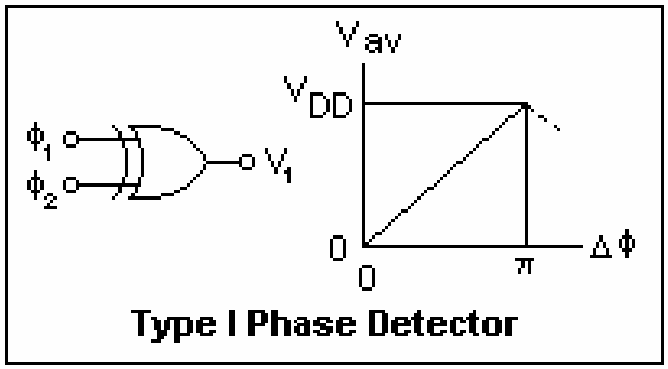


Loop Components

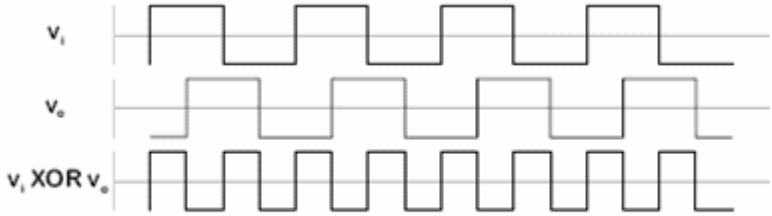
(1) Phase Detectors



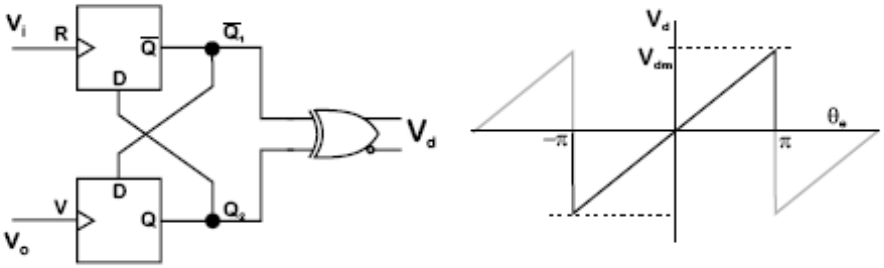
Whether or not a PLL can track a signal is largely dependent on the phase detector. This is the usual starting point for any PLL design. The simplest type, and a good one, is shown below. It is simply an exclusive-or (XOR) gate that gives a high output when the signals are of opposite sign, and a low output when they are of the same sign. When the signals are in phase, the output is 0, while if they are in antiphase, or with phase difference p radians, the output is a constant high value. If the two signals are of different frequency, the phase relation will change continuously, and the output will be a series of pulses. The effect on the VCO will be to change the frequency first one way, then the other, but in general the changes in the proper direction will be a bit longer, and will win out in the end, raising the VCO frequency to the input frequency. Then the phase relations are stable, and the delay is just enough to provide the average voltage necessary to the VCO. The two signals are brought to the same frequency, but not necessarily to the same phase. Nevertheless, the phase difference is constant.



XOR Phase Detector (Analysis):

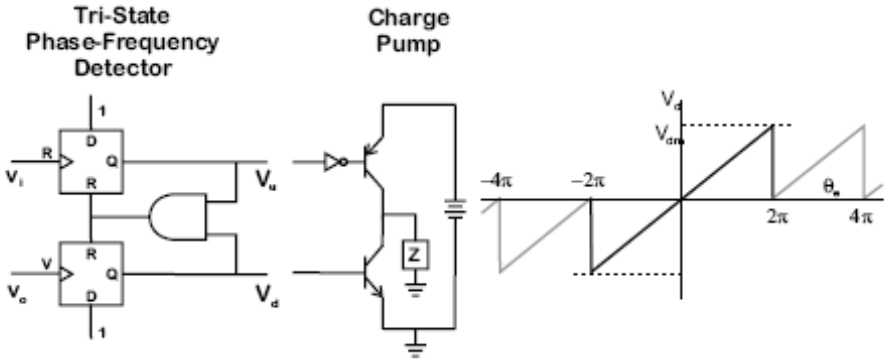


A 2 State Phase Detector:



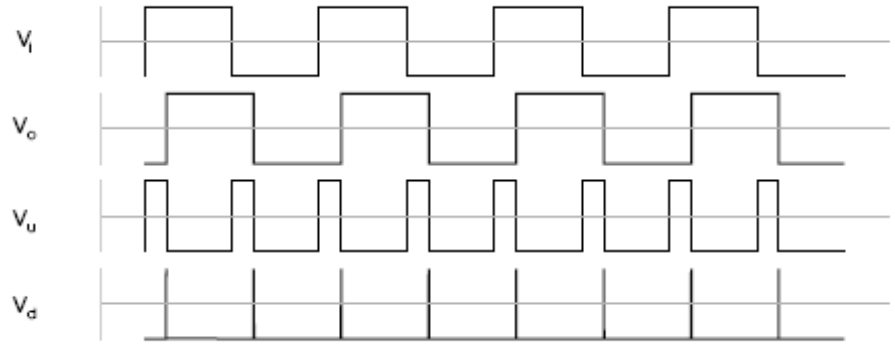
• Two state phase detection can be done using flip-flops as well as gates.
• The addition of the flip-flops adds memory to the system.
• The flip-flops are typically sensitive to only one clock edge, only the leading edges of the input and oscillator signals matter, not their duty cycles.
• The characteristic is a sawtooth.
• The memory elements desensitizes the PD to duty cycles, but makes it more sensitive to noise.

Phase-Frequency Detector:



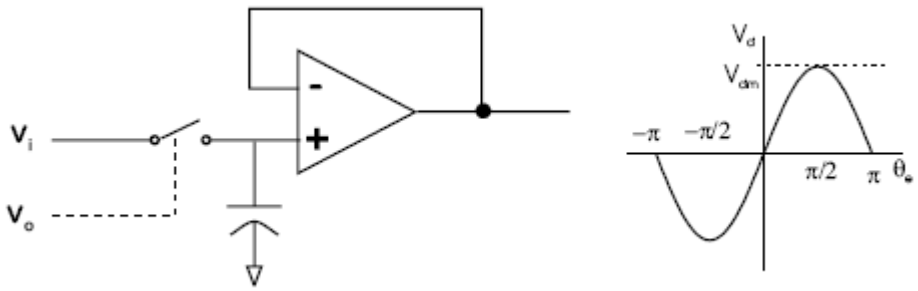
• It is a combination of a tri-state phase-frequency detector and a charge pump.
• The charge pump can be viewed as a 3 position switch controlled by the phase-frequency detector.
• The action of the charge pump is to alleviate any loading of the phase detector in driving the rest of the circuit. This allows the response to be smoother than without the charge pump.
• It is an extremely popular phase detector, used in frequency synthesis, motor control, etc.
• Note that the loop filter is often implemented in the Z block of the charge pump.
• Note that the 4*p* linear range is due to memory. PD can come up in one of 2 possible states and the PLL must account for this.

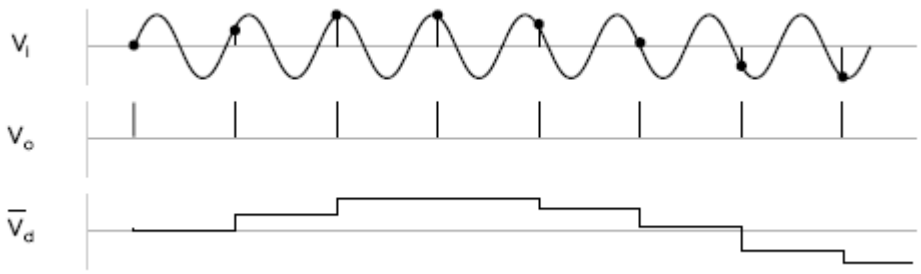
(Analysis)



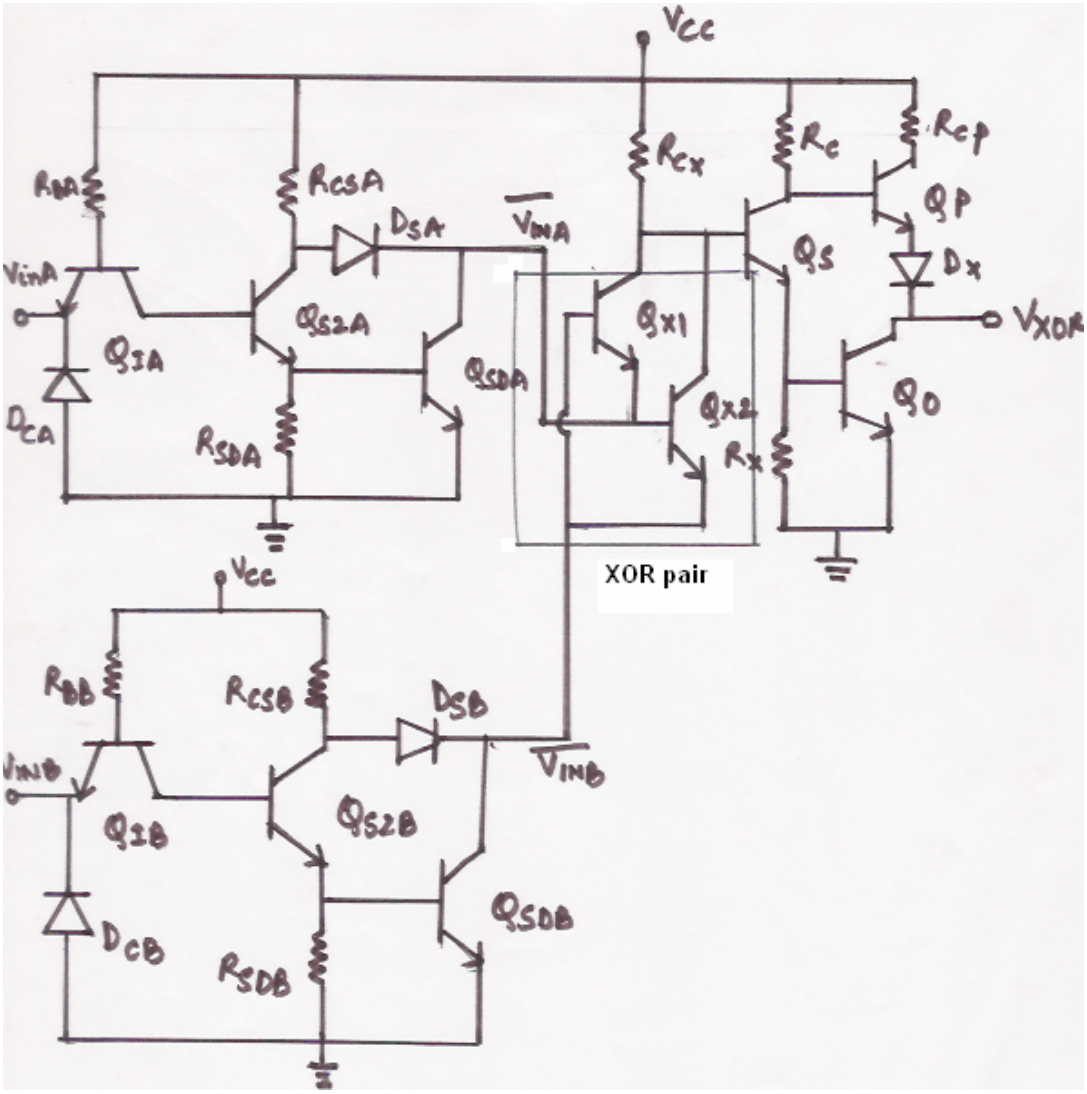
A small phase difference shows that only the leading edges of the signal and not the duty cycle are important.

Sample and Hold Phase Detector:





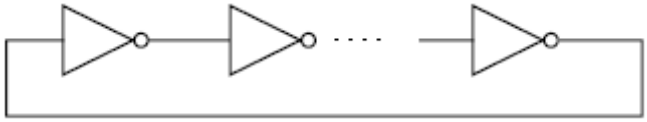
• The input signal, Vi is sinusoidal as shown in the right top plot.
• The VCO signal, Vo is used to trigger sampling of Vi as shown in the right middle plot.
• If the frequency of Vo matches or is close to the input frequency, the value of the sampled signal will depend only on the relative phase of Vi and Vo.
• Because the sample rate is below the Nyquist frequency, the samples alias down.
• These aliased samples create a phase error signal as seen in the right lower plot.
• The shape of the phase detector characteristic is based on the shape of the input signal, Vi, so that if Vi is sinusoidal, Vd is sinusoidal. If Vi is triangular, Vd is triangular. Finally, if Vi is a square/rectangular, then Vd has a relay characteristic.
• Note also that there is no high frequency component resulting from this phase detector. This can be seen analytically due to the fact that the zero-order hold has a zero at the sample frequency.


Vcc
RBA
RCSA
DSA
VINA
RCX
RC
RCP
QP
QS
DX
VXOR
VinA
QS2A
QX1
QSDA
QX2
QO
QIA
DCA
RSDA
RX
XOR pair
Vcc
RBB
RCSB
DSB
VINB
VinB
QS2B
QIB
QSDB
DCB
RSDB

(2) Voltage Controlled Oscillators:

Voltage controlled oscillator is a circuit that provides a varying output signal whose frequency is a function of input voltage.

Types of Oscillators which can be used as VCO:
• Ring Oscillator: common in monolithic topologies uses an odd number of inverters connected in a feedback loop.



• Relaxation Oscillator: uses a Schmitt-trigger to generate a stable square wave.

• Resonant Oscillator: puts a resonant circuit in the positive feedback path of a voltage to current amplifier.

• Other forms of VCOs, such as crystal oscillators and YIG oscillators essentially run on the same principle, but modify the resonant circuit.

VCO Circuit Design:

A simple design of VCO consists of a collector coupled astable multivibrator using n-p-n transistor with a control voltage.

Astable multivibrator is also known as free-running multivibrator. It has two quasi-stable states, and it makes periodic transitions between these two states. One of the transistors is normally ‘on’ and the other is normally ‘off’. The state of transistors changes continuously because of charging and discharging effect of the two capacitors C1 and C2.

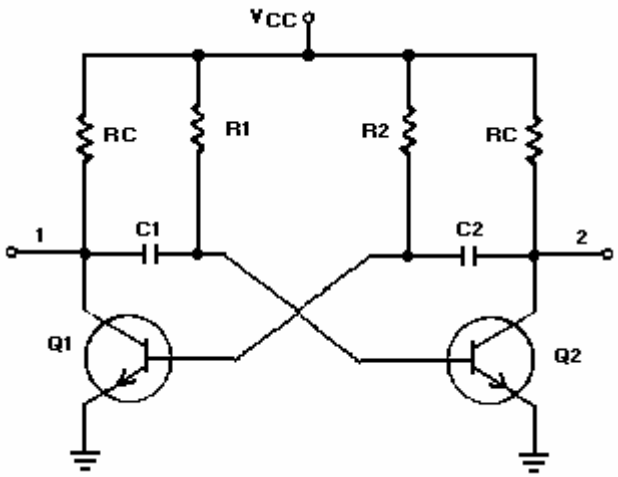


Fig (a)

The period of the output signal is given by,
T=1.38RC
when R1=R2=R and C1=C2=C
From the above equation it is clear that the frequency of oscillation may be varied over the range from cycles to megacycles per second by adjusting R or C.

To make this circuit work as 'voltage to frequency converter', it is slightly modified i.e. resistors R1 and R2 are given an auxiliary voltage V.

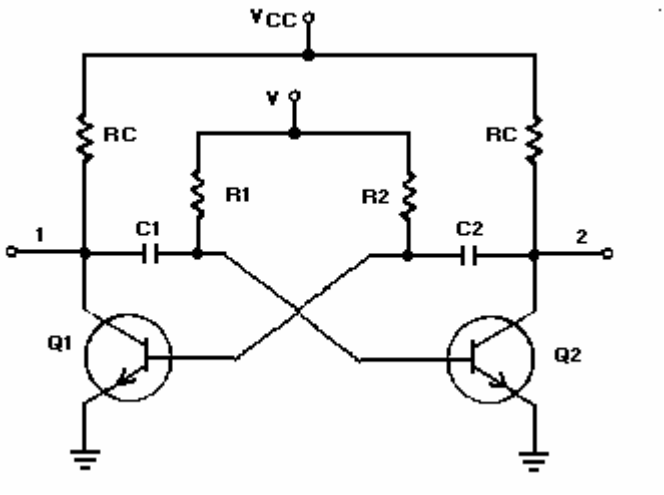


Fig (b)

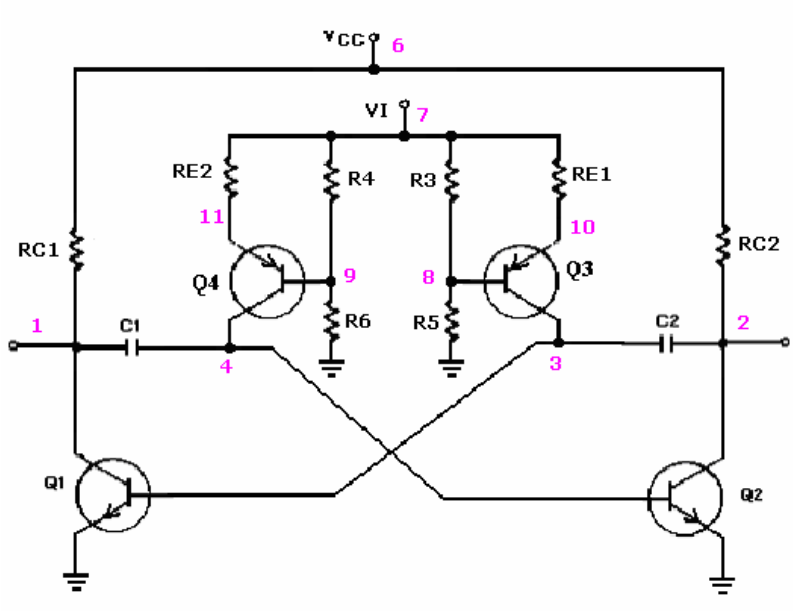
The output frequency now is controlled by the input voltage V and the relation is given by
f=1/2RCln (1+Vcc/V)

From the equation it is clear that the relation between the output frequency 'f' and input voltage 'V' is non-linear. To obtain a linear relationship between 'f' and 'V', the two resistors, R1 and R2, are replaced by transistors which act as constant current sources for charging C.

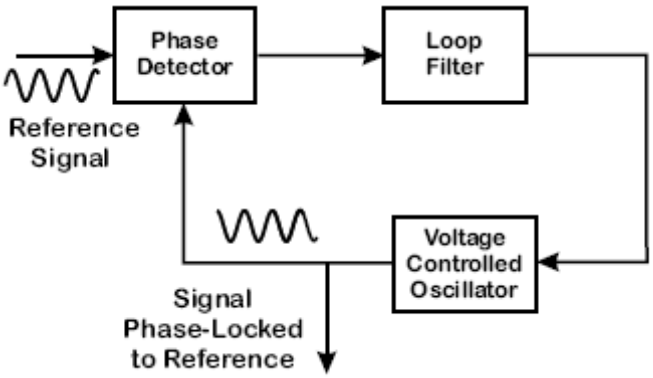
Phase Lock Loop Simulations

The modified circuit is shown below.

Fig

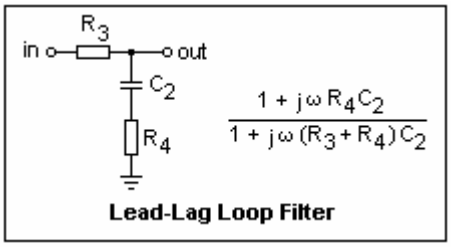


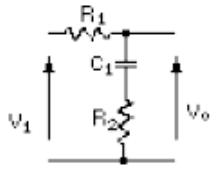
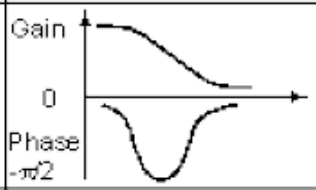
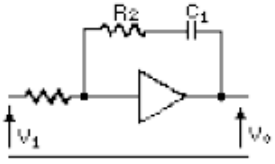
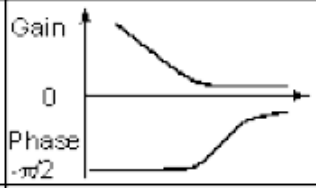
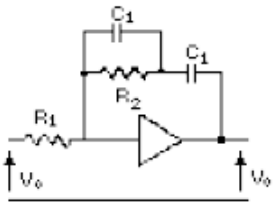
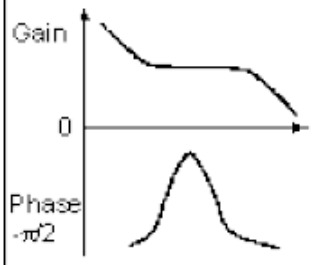
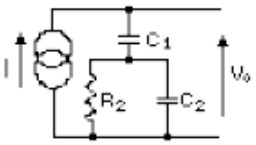
(3) Loop Filter:



• The loop filter is the one place where the designer really gets to shape the loop.
• Unfortunately, most filters are first order.
• Not many degrees of freedom here.
• This is where (as a rule) circuit designers seem to fall apart.

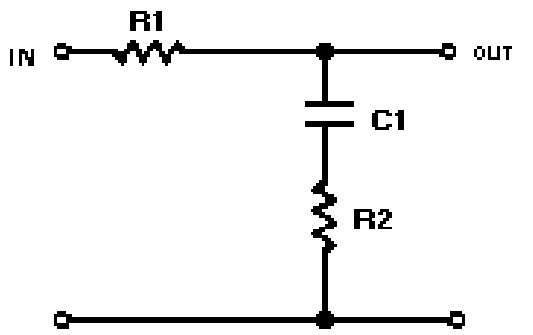
The simplest really satisfactory loop filter is the so-called lead-lag filter shown at the right. It is just an RC low-pass filter with an extra resistance in series with the capacitor. At low frequencies, its gain is 1, while at high frequencies it is a resistive divider with gain $R_4 / (R_3 + R_4)$. The frequency response function is said to have a *pole* at $2\pi f_c = 1/(R_3 + R_4) C2$ and a *zero* at $2\pi f_2 = 1/R_4C_2$. The pole provides a phase lead, while the zero a phase lag, so that the phase is zero both at low and high frequencies. It is easy to draw a Bode plot of the phase variation, as well as of the gain. One method of loop filter design is to determine satisfactory values for f_c and f_2, and then to proportion the filter reasonably. The resistors can be larger if the capacitor is smaller, and vice-versa. The values depend largely on the input resistance to the VCO; if this is high, anything goes, just about.



Element	Type	Transfer function	Time constants	
	lag/lead	$\frac{1 + sT_2}{1 + sT_1}$	$T_1=C_1(R_1+R_2)$ $T_2=C_1R_1$	
	Integrator & lead	$\frac{1 + sT_2}{sT_1}$	$T_1=C_1R_1$ $T_2=C_1R_1$	
	Integrator & lead/lag (phase comparator gives a voltage output)	$\frac{1}{sT_1}\ \frac{1 + sT_2}{1 + sT_3}$	$T_1=C_1R_1$ $T_2=R_2(C_1+C_2)$	
	Integrator & lead/lag (phase comparator gives a current output)	$\frac{1}{sC_1}\ \frac{1 + sT_2}{1 + sT_3}$	$T_3=C_2R_2$	

Transfer functions and bode diagram of various filter networks

Loop Filter Design Circuit:



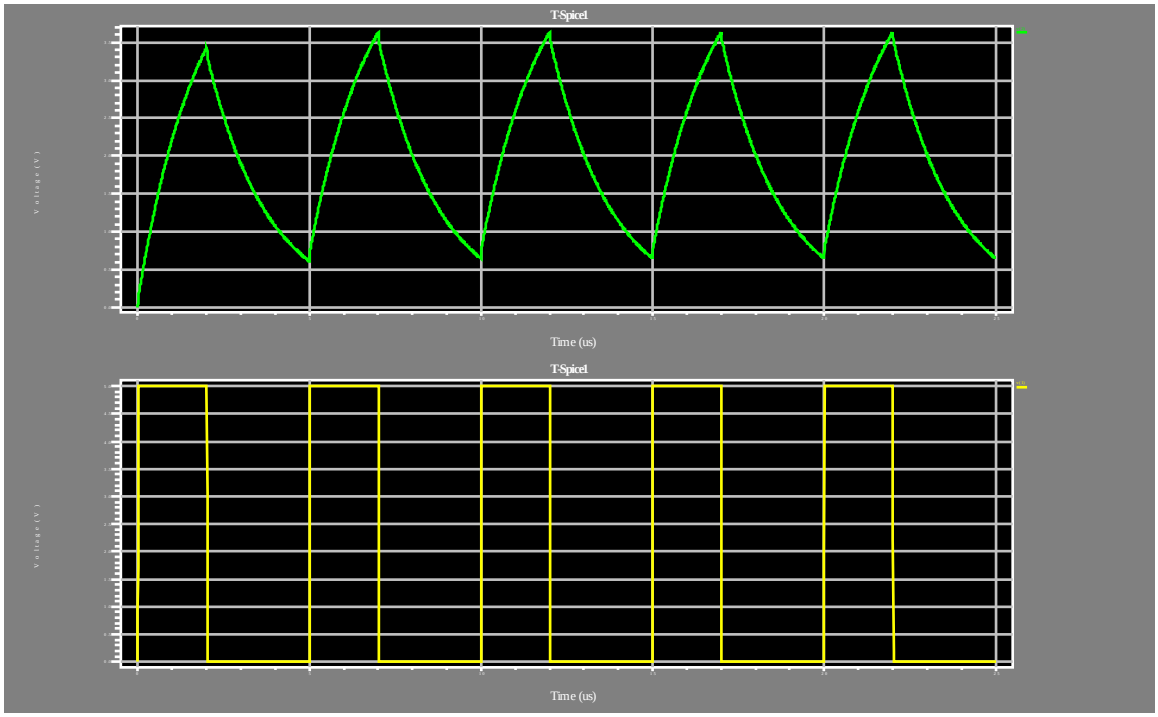
Hlp= (1+ sR2C1)/(1+ s(R1+R2)C1)

T-Spice code for the design circuits:

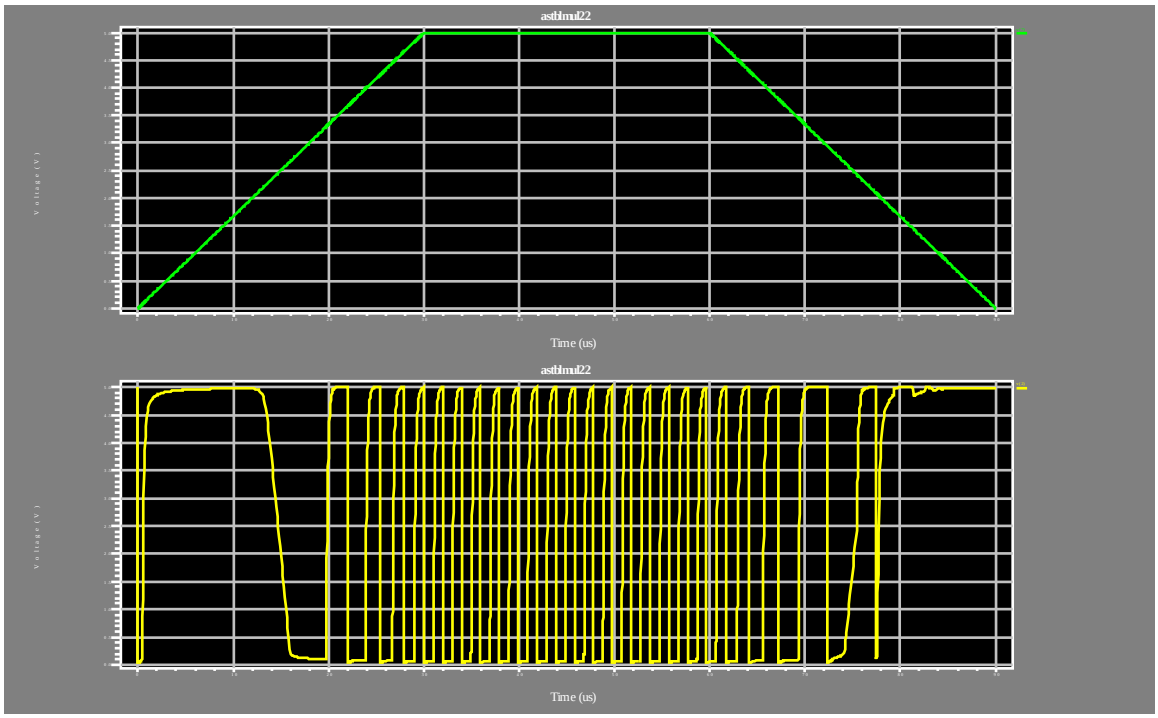
```
low pass filter
R1 1 2 86K
C1 2 3 20PF
R2 3 0 2K
VIN 1 0 PULSE(0V 5V 0US 0US 0US 2US 5US)
.TRAN 0.01US 25US
.PLOT TRAN V(1) V(2)
.END
Exor-gate for phase detector
VCC 4 0 5V
VINA 1 0 PULSE(0V 5V 0US 0.1US 0.1US 2US 5US)
VINB 9 0 PULSE(0V 5V 0US 0.1US 0.1US 3US 5US)
RBA 4 3 4K
RBB 4 8 4K
RCSA 4 5 1.9K
RCSB 4 11 1.9K
RSDA 7 0 1.2K
RSDB 12 0 1.2K
RCX 4 14 3K
RC 4 15 1.6K
RCP 4 16 120
RX 18 0 1K

DCA 0 1 DIODE
DCB 0 9 DIODE
DSA 5 6 DIODE
DSB 11 13 DIODE
DX 17 19 DIODE

Q1A 2 3 1 QM
Q1B 10 8 9 QM
QS2A 5 2 7 QM
QS2B 11 10 12 QM
QSDA 6 7 0 QM
QSDB 13 12 0 QM
QX1 14 13 6 QM
QX2 14 6 13 QM
QS 15 14 18 QM
QP 16 15 17 QM
QO 19 18 0 QM

.MODEL DIODE D (RS=40 TT=0.1NS)
.MODEL QM NPN (IS=1E-14 BF=50 BR=1 RB=70 RC=4 TF=0.1NS TR=1NS)
.TRAN 0.1US 15US
.PLOT V(1) V(9) V(19)
.END
```

```
astable multivibrator
VCC 6 0 DC 5V
VI 7 0 PULSE(0 5 0US 30US 30US 30US 40US)
RC1 6 1 1K
RC2 6 2 1K
RE1 7 10 1K
RE2 7 11 1K
R3 7 8 2K
R4 7 9 2K
R5 8 0 4.7K
R6 9 0 4.7K
C1 1 4 150PF
C2 2 3 150PF
Q1 1 3 0 QM
Q2 2 4 0 QM
Q3 3 8 10 QM1
Q4 4 9 11 QM1
.MODEL QM NPN (IS=2E-16 BF=50 BR=1 RB=5 RC=1 RE=0 TF=0.2NS TR=5NS)
.MODEL QM1 PNP (IS=2E-16 BF=100 BR=1 RB=5 RC=1 RE=0 TF=0.2NS TR=5NS)
.IC V(1)=0 V(3)=0
.TRAN 0.1US 90US
.PLOT TRAN V(2) V(7)
.END
```

Waveform Analysis:



Loop filter a) Output waveform b) Input wave



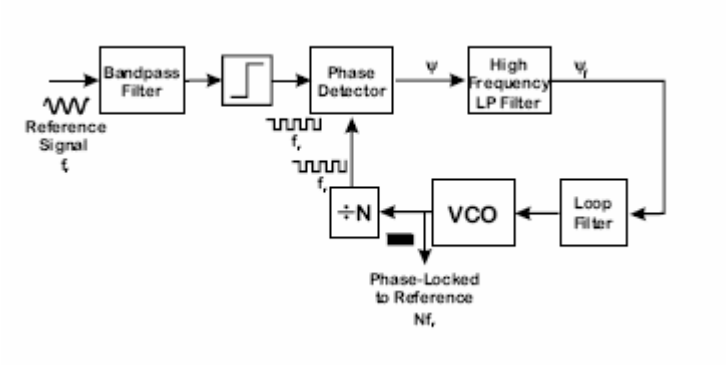
VCO waveform analysis showing the variations of output frequency with the input voltage

Applications

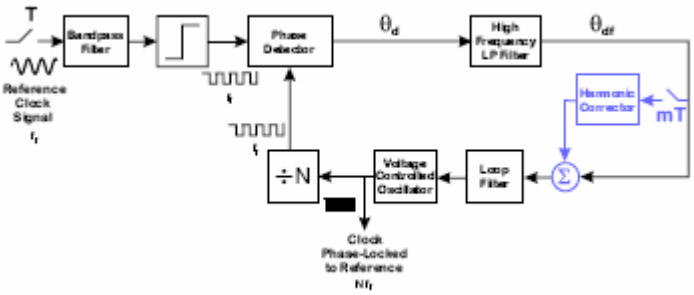
The reason that PLLs are so ubiquitous is that they are so useful in so many applications.

- Data and Tape Synchronization
- Modems
- Costas Loop
- FSK Modulation
- FM Demodulation
- Frequency Synthesizer
- Frequency Multiplication and Division
- Telemetry Receivers
- Signal Regeneration
- Satellite
- Robotics & Radio Control

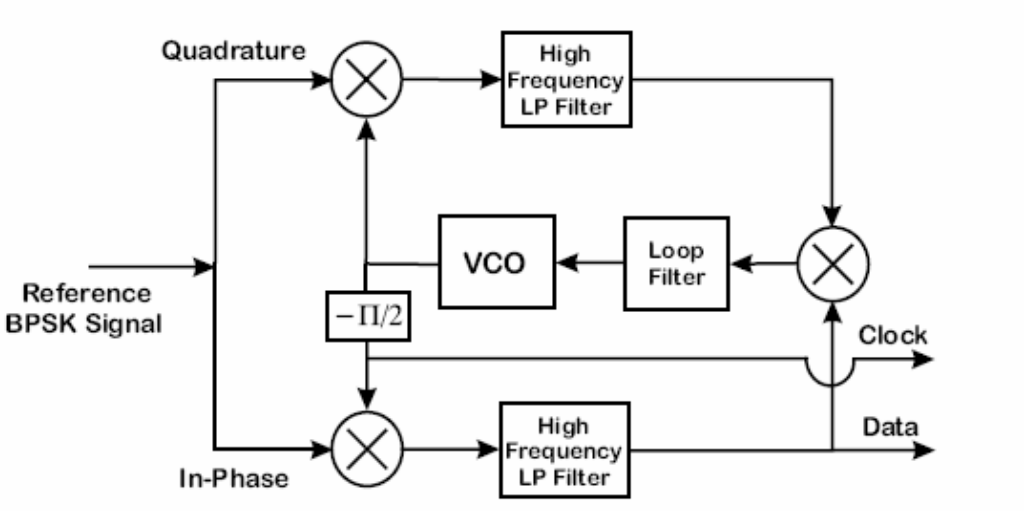
Frequency Synthesis:
• Want to lock a clock with an input signal of a different frequency.
• Synthesize a clock frequency from a lower frequency input.
• Harmonic locking loop generates a clock at N times input frequency.
• Non-integer N is possible.



• It is possible to remove harmonic phase modulation with a multi-rate harmonic corrector.



Costas Loop:



• A Costas loop can both recover the carrier and demodulate the data from such a signal.
• Intuitively, if there were no modulation, the upper arm is simply a PLL locks to a carrier.
• The effect of the lower arm of the loop is to lock to the modulation and cancel it out of the upper arm of the loop.
• It does the same thing as squaring loop, but down converts signal to baseband & does filtering there.
• Multiplier accomplishes same thing as squarer.

References:

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2. Thomas A. Demassa, Zack Ciccone *'Digital Integrated Circuits'*, John Wiley & Sons, 2001.
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4. Chen, Wai Kei, *'The VLSI Handbook'*, CRC Press LLC.
5. Muhammad H.Rashid '*SPICE for Circuits and Electronics Using PSpice'*, Prentice-Hall of India Pvt. Ltd, 2nd Edition.