Design and analysis of 10V 4-phase charge pump in ON Semiconductor C5 process.

Shaun A. Stickel

Abstract—A 4-phase charge pump designed using threshold voltage canceling circuits and a 4-phase voltage controlled oscillator driven clock. Input specification was 2.5V – 3.3V supply. Output specification was 10V with 100mV max ripple; up to 20pF capacitive load and up to 10µA load current. Physical design and layout was done using the 600nm ON Semiconductor C5 process.

I. ARCHITECTURAL OVERVIEW

The design of the charge pump has been broken down into four separate pieces: a clock generator, a buffer to drive the large capacitances of the pump, a 4 phase charge pump, and an output regulation and control circuit which regulates the output voltage to 10V and provides feedback to the clock generator.

The clock generator used a voltage controlled oscillator to generate a variable frequency clock; this clock was used as a source to a logic array that generated a 4 phase clock output. The oscillator frequency was controlled via feedback from the regulator section.

The pump was a 4 phase pump designed to eliminate losses between phases. Large buffers were needed to drive the clock inputs to the pump. This section could be easily scaled up or down depending on output loading requirements.

The regulator consisted of a class AB opamp in a voltage follower configuration acting as a linear regulator to set the output voltage to the desired level of 10V. There is an additional opamp used to send the analog control signals back to the clock generator which determines the output frequency of the oscillator.

II. CLOCK GENERATOR DESIGN

Clock generation was done by a digital circuit comprised of NAND gates and inverters which generate 4 clock signals referred to as phases. The output of this circuit (shown below) has been buffered by a chain of inverters to drive the inputs to the charge pump. A voltage controlled oscillator supplied the source clock for this circuit and was controlled by a differential analog voltage supplied to it from the control block.

In layout a methodology was used to make the process go more smoothly and to make debugging the layout easier. Each cell was constructed with a common height with PMOS devices on “top” and NMOS on “bottom”. The inputs and outputs of each cell were routed to the edge of the cell such that all cells could be placed adjacent to one another and no further routing would be needed. Metal3 was used only for power traces and all power connections in a cell go direct to metal3. Metal2 was used only for inter-cell routing or for special global signals going to and from a cell (i.e. the enable on the clocked inverter). Metal1 was used only for routing inside the cell or for cases where two signals on metal2 cross and one must go under the other, metal2 was not used inside the cell with the exception of global I/O connections.

III. CLOCK GENERATOR LAYOUT

Layout of the clock generator was done with a focus on minimizing area and parasitic delays, the full view of the layout is shown below. Cells were constructed for inverters,
clocked inverters, and NAND gates. A ring of clocked inverters formed the voltage controlled oscillator whose output was routed to a digital circuit which generated the four clock phases.

IV. BUFFER STAGE DESIGN

Each clock signal was buffered by a chain of 4 inverters with a fan-out of 3. The loading on phases 2 and 4 was less than that on 1 and 3, however, to preserve the phase to phase timing relationship all four phases used the same fan-out.

V. BUFFER STAGE LAYOUT

Buffer layout was based on the layout for the unit inverter and was done by increasing either the multiplier or width of the NMOS and PMOS by 3 for each step up size. Sizes of 3, 9, 27, and 81 were used.

VI. PUMP DESIGN

The charge pump itself was designed to be a threshold voltage canceling pump with four stages capable of generating voltages above the required 10V. The extra headroom was needed for the regulator to maintain the 10V output. Capacitor values were selected to ensure that the pump would be able to supply this voltage at 100µA loads. The sizing of charge transfer and bootstrap transistors was done using an iterative optimization process. The schematic below shows the design of the pump. A special bootstrap was added to keep the first phase of the pump at or above the supply voltage ensuring that all threshold voltage drops were removed from this design.

With a 7pF filter capacitor attached to the output of this pump (before the regulator section) the pump could supply a 100µA load with a ripple of less than 100mV and an output above 12V. Rise time of this pump under these conditions was less than 1us. This overhead guaranteed that process variations would not degrade performance to such a degree that the pump would not meet the specifications of the design.

VII. PUMP LAYOUT

The charge pump was laid out according to the schematic in a linear fashion. Cells were used for the 3pF and 300fF capacitors. Metal3 was used for power conduction because of its lower resistance.

IIIX. CONTROL DESIGN

Control and regulation was done in two pieces, one was a linear voltage regulator and the other a comparator going to a
current mirror to set the operating frequency of the voltage controlled oscillator.

The voltage regulator schematic is shown below. Sizing was found by experimentation, the current mirrors were set up to minimize excess loading on the pump.

The comparator (provided for this project by the course instructor) controlled a current mirror to put the oscillator in either "turbo" or "normal" mode. This allowed the pump to have a fast startup time and a lower power consumption when running in steady state at currents above the required 10µA.

The comparator layout and control schematic are shown below.

IX. CONTROL LAYOUT

The control system was laid out in two sections, the comparator and the voltage regulator section.

X. SIMULATION RESULTS

Simulation of the circuit was done based on extracted view first priority for the system. Data was taken for "worst case" scenarios for each parameter specified in the project specification. Additionally data points were taken for different process corners.

Worst case rise time was seen with 10µA load and 20pF output capacitance. Worst case ripple was found with 10µA load and no output capacitance. Output voltage was checked at no load and 10µA load. The following are graphs of the pumps output at a nominal process corner.

At nominal process corner the pump had a rise time of less than 2.5µs with a 10µA load and a 20pF load capacitance. The ripple seen with a 10µA load and no load capacitance was less than 90mV.

Simulation results for other process corners are shown in the table below.
According to these simulation results, the pump meets the project specifications at nominal, however, at process corners the voltage ripple does not meet specifications.

Running the pump at an input voltage of 2.5V with a nominal process corner yielded the following results.

<table>
<thead>
<tr>
<th>Corner</th>
<th>$T_{rise}$</th>
<th>$V_{ripple}$</th>
<th>$V_{out,0\mu A}$</th>
<th>$V_{out,10\mu A}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>nom</td>
<td>2.5\mu s</td>
<td>88mV</td>
<td>10.63V</td>
<td>9.998V</td>
</tr>
<tr>
<td>fnfp</td>
<td>2.0\mu s</td>
<td>103mV</td>
<td>10.57V</td>
<td>9.974V</td>
</tr>
<tr>
<td>fnsp</td>
<td>2.0\mu s</td>
<td>103mV</td>
<td>10.59V</td>
<td>9.974V</td>
</tr>
<tr>
<td>snsp</td>
<td>2.5\mu s</td>
<td>154mV</td>
<td>10.63V</td>
<td>9.971V</td>
</tr>
<tr>
<td>snfp</td>
<td>2.2\mu s</td>
<td>111mV</td>
<td>10.66V</td>
<td>9.968V</td>
</tr>
</tbody>
</table>

Table of simulation results across process corners

The slowdown in rise time was due to the voltage controlled oscillator's sensitivity to supply voltage variation. The lower output voltage is likely due to supply voltage dependencies in the regulator and the fact that the boost of each stage in the charge pump was much less at a supply voltage of 2.5V.

Additionally operating the pump and different temperatures yielded the following results.

<table>
<thead>
<tr>
<th>Corner</th>
<th>$T_{rise}$</th>
<th>$V_{ripple}$</th>
<th>$V_{out,0\mu A}$</th>
<th>$V_{out,10\mu A}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V</td>
<td>2.5\mu s</td>
<td>88mV</td>
<td>10.63V</td>
<td>9.998V</td>
</tr>
<tr>
<td>2.5V</td>
<td>30\mu s</td>
<td>126mV</td>
<td>8.40V</td>
<td>8.55V</td>
</tr>
</tbody>
</table>

Table of results for 2.5V supply voltage

The robustness of the regulation stage was evaluated by using a pulse current source transitioning between 0\mu A and 10\mu A with 10ns rise and fall times and no load capacitance, the resulting graph (at nominal process corner) is shown below.

Plot of output voltage with pulse load from 0\mu A to 10\mu A

XI. CONCLUSIONS

The design as a whole was able to meet the design requirements only at nominal conditions, this indicates that some additional circuitry to help eliminate supply voltage and process dependencies would be a great help to the design. Additionally the output ripple was the biggest problem when evaluating across process corners, therefore an improved regulator or addition of a filter would be beneficial.