High Efficiency and Low Noise Charge Pump Circuits for Non-volatile Memories

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Abstract

Along with the System-on-Chip (SoC) concept being widely adopted, more and more building blocks are to be implemented into one chip. However, those different building blocks are generally not all specified with the same supply voltage, for example, 1.8V for the digital parts while 3.3V for the analog parts in most 0.18µm products. Generally, Low-Dropout (LDO) regulators are used to solve the problem at the cost of efficiency if all the required voltages are below the supply. On the other hand, switching regulators is able to provide both higher and lower voltages with very high efficiency, but the need for an inductor makes it quite area consuming and the efficiency drops tremendously in light load condition. Besides, the control loop also requires very sophisticated design. Whereas the charge pump circuit, owning to its relatively compact size and simple control strategy, has earned lots of attention in applications where an on-chip high voltage supply with relatively low output current is much preferred. Especially in non-volatile memories such as EEPROM or NAND flash, the performance is heavily dependent on the charge pump circuit which provides the required programming or erasing high voltage, usually more than 10V.

In recent years, since the stringent power budget of LSIs is continuously squeezing the supply voltage, two main challenges arise for the charge pump circuit design in non-volatile memory. The first challenge is related to the power efficiency. As the supply voltage of non-volatile memory scaling down, the stage number of the charge pump circuit must be increased, since the programming voltage is defined by the energy gap physically and is not likely to be lowered in the same way. As a result, the power penalty for the extra stages and
the saturation effect caused by transistors’ body effect deteriorates
the efficiency, which becomes a very serious problem for those appli-
cations powered by batteries. Although many new structures have
been worked out to improve the output linearity with respect to the
stage number, the dynamic power loss problem due to the parasitic
capacitance is seldom touched. The second challenge is related to the
output noise. For non-volatile memory, lowering the operating voltage
also means shrinking the threshold window and the noise margin as
well. This makes the memory cell more sensitive to the programming
noise, and thus more verifying process is required to correct the error
at the cost of memory data throughput. Conventional noise suppress-
sion method relies on increasing the output decoupling capacitance,
while the large area overhead and the slow setup time is prohibitive
for many applications.

This thesis is mainly written to address the above two problems
based on the analysis and experiments. The basic knowledge of MOS
transistor and analog circuit will not be restated, while the impact of
some secondary effects is to be analyzed. The charge pump circuit
is introduced by its application in non-volatile memory. The basic
operation with the mathematical model will be derived step by step
to provide a reference for the analysis of more in-depth problems.
Different charge pump structures are also briefly described for com-
parison. Although there might be some overlapping, the charge pump
efficiency and noise problems in this thesis will be discussed separately
and independently. Detailed theoretical analysis is presented and the
measurement results are given to prove the validity of the proposed
solutions.

Chapter 1 begins with the introduction of the non-volatile memory,
and explains the role and importance of the charge pump circuit. The
utilization of the charge pump circuit in other applications is also
briefly mentioned. The main topics in this thesis are also clarified.
Chapter 2 describes the basic operation of the charge pump circuit. The mathematical model is derived and the influence of the charge transfer unit is analyzed in detail. The conventional Dickson charge pump and the four phase clock scheme is also introduced with the simulation results.

Chapter 3 concentrates on the design of a better charge transfer unit based on the analysis of chapter 2. The threshold voltage and body effect cancellation scheme are explained. A switched polarity charge pump is designed with the proposed charge transfer unit, and the simulation results with comparison are shown as well.

Chapter 4 deals with the efficiency problem for low voltage supply. The charge pump efficiency is analyzed, and the influence of the bottom-plate parasitic is emphasized. A complementary charge pump architecture with charge sharing clock scheme is proposed to recover part of the dynamic loss during the pumping process, and the charge sharing order can be double or triple. A charge pump circuit with double charge sharing clock scheme is fabricated in 0.18 µm technology with a parasitic ratio of 0.1, and the measurement results shows more than 10% peak efficiency increase with no drivability decline. The proposed triple charge sharing clock generator is able to recover nearly two-thirds of the charge from the parasitics charging, in which way the dynamic power loss in the pumping process is reduced to almost one-third. Under 0.18 µm technology with a bottom plate parasitic ratio of 0.2, the simulation results show an overall efficiency increase with a peak value of 62.8% comparing to 46.8% of a conventional one, and the output ripple voltage is reduced by nearly a half.

Chapter 5 deals with the output noise of the charge pump circuit. Different noise suppression methods are first introduced and their limitations are described. The output noise is then re-analyzed in spectrum domain. A hybrid decoupling scheme using both active decoupling and passive decoupling method is proposed to suppress the
noise power without output capacitance increase. The mathematical model of the proposed scheme is carefully derived, and a fast optimization method is given to balance the active and passive decoupling path so that a maximum decoupling performance is able to be achieved. Test chip is also fabricated in 0.18$\mu$m technology. The measurement results shows more than 15.4dB noise suppression improvement with the same output capacitance.

Chapter 6 concludes the thesis and gives the prospect on future design concerns.
To my beloved parents and my wife
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<td>Channel Hot-Electron Programming</td>
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<td>CP</td>
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<td>CTU</td>
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<td>EEPROM</td>
<td>Electrically Erasable Programmable Read-Only Memory</td>
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1

Introduction

The charge pump circuit is used to generate a voltage higher (positive charge pump) or lower (negative charge pump) than the voltage supply. It is one of the most important building blocks in the non-volatile memories, because the programming and erasing operation are fully dependent on the charge pump circuit.

In this chapter, we mainly introduce the charge pump circuit through its application in non-volatile memory to show readers a direct impression. The detailed circuit configuration and operation principle are described in the next chapter.

1.1 Charge Pump Circuits in Non-volatile Memories

Semiconductor memory is an essential part of modern information processors, and it has been more or less growing in both density and performance in accordance with Moore’s Law. Semiconductor non-volatile memory technology, as a major subset of solid-state memory, has made lots of progress and is gaining increased interest during these years.

Non-volatile memory, as the name indicates, is a memory that can retain the stored information even when not powered. Each non-volatile memory technology
1. INTRODUCTION

exploits some physical or chemical approach to capture and retains a representation of information independent of the presence of a power. According to the storage mechanism, they can be generally categorized into floating-gate devices like NAND flash, charge-trap devices like SONOS, and phase-change devices.

Take the floating-gate device for example, which is commonly used for NAND flash memory, the basic structure is shown in Fig. 1.1-a. The floating-gate device is similar to a normal MOSFET transistor except that it has a floating gate (FG in Fig. 1.1-a) surrounded by the insulators between the control gate (CG) and the P-well. Suppose a sense voltage is applied to the control gate CG with no charge stored in the floating-gate FG, the current will flow as long as the source to drain voltage is not zero, just like the operation of a normal transistor. However, if some charge is stored in the floating-gate, the negative electrical field will counter-act with the positive field generated by the control gate voltage at the surface of the channel. As a result, the control gate voltage must be increased to maintain the current flow. Namely, the threshold voltage $V_{th}$ of such device is changed according to the charge quantity $Q$ stored in the floating-gate FG, and the relationship is expressed as:

$$V_{th} = K - Q/C_{ox},$$

where $K$ is a constant depending on the gate and substrate material, channel doping and gate oxide thickness, $C_{ox}$ is the gate oxide capacitance between CG

---

**Figure 1.1:** Floating gate NVM with program and erase scheme ($V_{dd} = 3V$).
According to the quantum mechanics, a lot of energy is required to program (inject electron into FG) or erase (remove electron from FG) the cell. Basically, there are two mechanisms. One is called the Fowler-Nordheim (F-N) Tunneling \[5\], and the other is called the Channel-Hot-Electron (CHE) Injection \[6\], both require voltages much higher than the supply. Based on these two mechanisms, two kinds of programming schemes are shown in Fig.1.1-b, and two kinds of erasing schemes in Fig.1.1-c, and according to Eq.1.1, The I/O characteristic of the programmed and erased cell are shown in Fig.1.1-d. Once the cell is programmed, it can be read by applying a moderate voltage (dotted line in Fig.1.1-d) on the control gate CG and sense the output current. If no current flows, a "0" is read, and if the current flows, a "1" is read.

The operation principle of NVM seems to be simple, but getting enough energy to program and erase the cell requires a voltage much higher than the supply voltage as shown in Fig.1.1-b,c, for example 15V at the 3V supply \(V_{dd}\) or even lower. In the early years of the NVM, the high voltage is mostly provided from the outside circuit which is huge in size. It was unimaginable that the NVM can be used for mobile device until the come-out of charge pump circuit, which is constructed with only transistors and capacitors and is able to be fully implemented.
1. INTRODUCTION

on-chip. After years of technology development and circuit design improvement, it has now become the most important building block in all NVM architectures, which is shown in Fig.1.2.

1.2 Charge Pump Circuits in Other Applications

The usage of charge pump circuit also extends to other applications such as DRAM. A standard DRAM cell is composed of a NMOS transistor and series connected charge storage capacitor. The standard structure is shown in Fig.1.3.

The charge is preserved in the capacitor (C in Fig.1.3) when the word line (WL in Fig.1.3) is low, and dynamic refresh operation is essential to prevent error caused by the leakage current. There is a strong relationship between the leakage current and the NMOS threshold $V_{th}$, which is expressed in Eq.1.2 and Eq.1.3 that

$$I_{leak} \propto e^{-\alpha V_{th}}, \quad (1.2)$$
$$V_{th} = V_{th0} + \gamma \left( \sqrt{2 \Phi_F} + V_{SB} - \sqrt{2 \Phi_F} \right), \quad (1.3)$$

where $\alpha$ is a constant, $V_{th0}$ is the zero-biased threshold, $V_{SB}$ is the source-body bias, $\gamma$ is the body effect coefficient and $\Phi_F$ is the substrate Fermi potential. Clearly, the most effective way to suppress the leakage current is increasing the
V_{SB}, namely, dropping the NMOS bulk bias to negative when the data is preserved. In single supply DRAM architecture, negative charge pump is used to generate the required negative voltage. In this manner, the leakage current is effectively suppressed, the refresh period can be longer, and the power consumption also decreases.

Besides, charge pump circuits are also widely adopted in other situations. A common problem in system engineering is that the subsystem power requirements are not met by the main supply, in such cases, charge pumps can be an option. For the gradually declining voltage of a discharging battery, charge pumps can be used to maintain the voltage level. In addition, charge pumps can be the only choice for certain applications, such as telecommunication devices, which are extremely sensitive to electromagnetic interference.

1.3 Main topics in this thesis

In recent years, since the stringent power budget of LSIs is continuously squeezing the supply voltage, two main challenges arise for the charge pump circuit design in non-volatile memory. The first challenge is related to the power efficiency. As the supply voltage of non-volatile memory scaling down, the size of charge pump circuit (stage number) must be increased, because the programming voltage is defined by the energy gap physically and is not likely to be lowered in the same way. As a result, the power penalty and the saturation effect caused by transistors’ body effect deteriorates the efficiency, which becomes a very serious problem for those applications powered by batteries. Although many new structures have been worked out to improve the output linearity with respect to the stage number, the dynamic power loss problem due to the parasitic capacitance is seldom touched. The second challenge is related to the output noise. For non-volatile memory, lowering the operating voltage also means shrinking the threshold window and the noise margin as well. This makes the memory cell more sensitive to the programming noise, and thus more verifying process is required to correct the error, however, this not only influences memory data throughput but also deteriorates the endurance. Conventional noise suppression method relies on in-
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Increasing the output decoupling capacitance, while the large area overhead and the slow setup time is prohibitive for many applications.

This thesis is mainly written to address the above two problems based on the analysis and experiments. The basic knowledge of MOS transistor and analog circuit will not be restated, while the impact of some secondary effects is to be analyzed. The basic operation with the mathematical model will be derived step by step to provide a reference for the analysis of more in-depth problems. Different charge pump structures are also briefly described for comparison. Although there might be some overlapping, the charge pump efficiency and noise problems in this thesis will be discussed separately and independently. Detailed theoretical analysis is presented and the measurement results are given to prove the validity of the proposed solutions.
In this chapter, we will introduce the structures of the charge pump circuits, and explain how the high voltage is generated. We start with a most simple charge pump model and derive the mathematical model. Further analysis is also included to better understand the charge pump property. Then, conventional charge pumps are introduced and analyzed as examples to show some common problems in the charge pump circuit design.

2.1 The Charge Pump System

A basic block diagram of the charge pump system is shown in Fig. 2.1. It consists of three sub-blocks: the clock driver, the N-stage charge pump and the voltage regulator. The clock driver generates the desirable clock schemes to feed the
2. CHARGE PUMP ANALYSIS AND TYPICAL STRUCTURES

charge pump. In some charge pump circuits which require precise clock control to achieve high efficiency, this block is very important and should be carefully designed. For those other charge pumps with simple control, this block is not necessary if a suitable system clock is available. The N-stage charge pump is responsible for generating the high voltage. It is the core of the charge pump system, and can be completely different according to the system requirement. In some cases, there may even be $m$ parallel N-stage charge pumps in order to provide more output current. The Voltage regulator, usually composed by voltage divider and comparator, maintains the output voltage at the target level. This block is related to the output noise issue, and is important for mix-signal applications.

Other control blocks can also be added to the system, if more additional functions are desired.

2.2 The N-Stage Charge Pump Model

Despite of the various forms of charge pump circuits, they are always derived from the same architecture shown in Fig.2.2.

Each node of the diode chain is coupled to the input clocks via capacitors in parallel. The diodes work as one-way valves so that the charge stored in the capacitors can not flow back to the input. $\phi$ and $\bar{\phi}$ are two out-of-phase clocks, and are attached to capacitors reciprocally. The charge pump operates by pumping charge packets along the diode chains as the coupling capacitors are successively charged and discharged each half-clock cycle. Since the voltage are not reset after each pumping cycle, the average node potentials increase progressively from the input to output of the diode chain.

For the first stage from $V_{in}$ to $V_1$, capacitor $C$ is charged during the time $\phi$ is low until the potential reaches $V_{in} - V_D$, in which $V_D$ is the forward bias diode voltage. And when $\phi$ goes high, if there is no current output, the potential becomes

$$V_1 = V_\phi - V_D + V_{in},$$  \hspace{1cm} (2.1)
2.2 The N-Stage Charge Pump Model

Figure 2.2: N-stage charge pump architecture and the wave form.

where $V_\phi$ is the clock amplitude, as shown in Fig.2.2. In the same manner, the difference between the voltages of the $n$th and $(n+1)$th nodes at the end of each pumping cycle is given by

$$\Delta V = V_{n+1} - V_n = V_\phi - V_D.$$  

(2.2)

Thus, for $N$ stages, the voltage at $N$th node can be represented as

$$V_N = V_{in} + N(V_\phi - V_D),$$

(2.3)

and since the last diode isolates the output node from the $N$th node, the output voltage of an N-stage charge pump is obtained as

$$V_{out} = V_{in} + N(V_\phi - V_D) - V_D.$$  

(2.4)

This equation shows the output voltage in an ideal situation when the pump is not delivering any output load current, namely $I_{out} = 0$. Because the pump will
be connected to an output load $R_L$ and there is a load current, the output voltage will not remain at that expressed in Eq.2.4. Assuming $V_{\text{drop}}$ as the voltage drop per stage for supplying the load, the charge pumped by each stage per clock cycle is $CV_{\text{drop}}$. If the clock frequency is $f$, the current supplied by the charge pump is given by

$$I_{\text{out}} = fCV_{\text{drop}}.$$  

(2.5)

Rearranging Eq.2.5, the voltage drop for each stage is

$$V_{\text{drop}} = \frac{I_{\text{out}}}{fC}.$$  

(2.6)

Rewriting Eq.2.4 by incorporating Eq.2.6, the output of N-stage charge pump becomes

$$V_{\text{out}} = V_{\text{in}} + N(V_\phi - V_D - \frac{I_{\text{out}}}{fC}) - V_D.$$  

(2.7)

Because the current is not delivered constantly to the load $R_L$, a voltage ripple $V_r$ occurs when $\bar{\phi}$ goes low, which is expressed as

$$V_r = \frac{V_{\text{out}}}{fR LC_L}.$$  

(2.8)

This ripple voltage is the noise to the loading circuits. Large ripple may affect the operation of chip such as PLL, EEPROM or flash memory. In real applications, a most common way to suppress the ripple noise is to choose a large $C_L$, but this may bring other problems. We will go back to this point in the later chapter.

2.2.1 Further Analysis

The basic operation of a N-stage charge pump has been briefly explained in previous section. If we further analyze the model, more useful property can be revealed.

First of all, recall Eq.2.7, if $V_{\text{in}}$ and $V_\phi$ equal to the supply voltage $V_{dd}$ ($V_{\text{in}} = V_\phi = V_{dd}$), there is no output current ($I_{\text{out}} = 0$), and the diodes are all ideal ($V_D = 0$), we define the output of a N-stage charge pump in such situation as the ideal output, given by

$$V_{\text{ideal}} = (N + 1)V_{dd}.$$  

(2.9)
2.2 The N-Stage Charge Pump Model

This indicates a theoretical limit that a N-stage charge pump can ever achieve. The more close the un-loaded output to this value, the more efficient the charge pump is.

In Eq.2.7, we should notice that the following equation must be satisfied to guarantee that the charge pump works properly.

\[ V_{\phi} - V_D - \frac{I_{out}}{fC} > 0. \] (2.10)

If Eq.2.10 does not stand, the output voltage does not increase even if more stage is added.

Notice that Eq.2.7 can also be rewritten as

\[ V_{out} = V_s - I_{out}R_s, \] (2.11)

where

\[ V_s = V_{in} + N(V_{\phi} - V_D) - V_D, \] (2.12)

\[ R_s = \frac{N}{fC}. \] (2.13)

According to Eq.2.11, the charge pump shown in Fig.2.2 can be replaced by the equivalent model of Fig.2.3. And by solving the RC network, the output voltage to time can be obtained as

\[ V_{out}(t) = V_s \left[ 1 - e^{-\frac{t}{\tau_{out}} \cdot fC} \right]. \] (2.14)
2. CHARGE PUMP ANALYSIS AND TYPICAL STRUCTURES

Then, the set up time $t_{\text{setup}}$ for the charge pump output rising from 0 to $V_{\text{out}}$ can be easily calculated, which is

$$t_{\text{setup}} = (R_s \parallel R_L)C_L \cdot \ln \left( \frac{V_s}{V_s - V_{\text{out}}} \right).$$

(2.15)

If $V_{in} = V_\phi = V_{dd}$ and $R_s \ll R_L$, a simpler form can be achieved as

$$t_{\text{setup}} = \frac{NC_L}{fC} \cdot \ln \left[ \frac{(N + 1)(V_{dd} - V_D)}{(N + 1)(V_{dd} - V_D) - V_{\text{out}}} \right].$$

(2.16)

We have learned the basic operation of a charge pump and some of the important properties. However, the analysis by is based on the N-stage charge pump prototype shown in Fig. 2.2, which is an ideal mathematic model. In real circuit implementation, the situation is more complex, and more factors should be taken into consideration, such as parasitics and device endurance.

2.3 Dickson Charge Pump

The first circuit implementation of the model shown in Fig. 2.2 is the Dickson charge pump [1] shown in Fig. 2.4. The only difference is replacing the diodes by diode connected NMOS transistors.
2.4 NMOS Four Phase (N4P) Charge Pump

The output voltage of a Dickson charge pump can thus be expressed in the same manner as Eq. 2.7

\[ V_{out} = V_{dd} - V_{th}(0) + \sum_{n=1}^{N} \Delta V(n), \quad (2.17) \]

where \( \Delta V(n) \) is the pump gain, \( V_{th}(n) \) is the NMOS threshold voltage of the \( n \)th stage with body effect

\[ \Delta V(n) = \frac{CV_{dd}}{C + C_s} - V_{th}(n) - \frac{I_{out}}{(C + C_s)f}, \quad (2.18) \]

\[ V_{th}(n) = V_{th0} + \gamma \left( \sqrt{2\Phi_F + V_{SB}(n)} - \sqrt{2\Phi_F} \right), \quad (2.19) \]

where \( C_s \) is parasitic capacitance and \( f \) corresponds to the operation frequency. \( I_{load} \) is the output current if there is any load. \( V_{th0} \) is the zero-biased threshold, \( V_{SB}(n) \) is the \( n \)th stage source-body bias, \( \gamma \) is the body effect coefficient and \( \Phi_F \) is the substrate Fermi potential.

The maximum output voltage \( V_{max} \) is obtained when the stage gain \( \Delta V(n) = 0 \), and combining Eq.2.18 and Eq.2.19:

\[ V_{max} = \left( \frac{V_{dd} - V_{th0}}{\gamma} + \sqrt{2\Phi_F} \right)^2 - 2\Phi_F. \quad (2.20) \]

The main draw back of the Dickson charge pump is the low stage gain caused by diode connected NMOS, and is even deteriorated by the body effect. The limited output voltage also restricts the performance.

### 2.4 NMOS Four Phase (N4P) Charge Pump

To overcome the draw back of Dickson charge pump, many new techniques and architectures have been reported [2, 3, 7, 8, 9, 10, 11, 12, 13], and the NMOS four phase (N4P) charge pump [3] is the most classic example among them.

A 3-stage N4P charge pump is shown in Fig. 2.5. The most important feature of this structure is the gate boost scheme, usually called the threshold voltage cancellation scheme. Many other architectures [8, 10, 12] utilize this technique to achieve high performance. The idea is to boost the gate of a charge transfer
2. CHARGE PUMP ANALYSIS AND TYPICAL STRUCTURES

MOS transistor to higher potential, so that its drain and source can reach the same potential.

2.4.1 Threshold Voltage Cancellation scheme in N4P

In this section, we explain the operation of threshold voltage cancellation in N4P. And we take the second stage in Fig. 2.5 for example.

As shown in Fig. 2.5, one period clock can be divided into four steps: $S_1, S_2, S_3$ and $S_4$. In $S_1$, $\varphi_1$ and $\varphi_3$ is low while $\varphi_2$ is high, then transistor $M_g$ is turned on, making $n_1$ and $n_g$ short. This means transistor $M$ is diode connected, and no charge can flow back from $n_2$ to $n_1$. This corresponds to the charge hold stage.

In the following $S_2$, $\varphi_1$ goes high bringing $n_1$ high. Because $M_g$ is on, $n_g$ will be brought to nearly the same potential as $n_1$.

In $S_3$, $\varphi_2$ goes low to turn off $M_g$, then $\varphi_3$ rises to high. Since $n_g$'s potential has been raised to the same as $n_1$ in $S_2$, it is now higher than $n_1$. The relation...
amount $n_1, n_2$ and $n_g$ can be expressed as:

$$V_{ng} = V_{n1} + \alpha V_{dd} > V_{n1} > V_{n2},$$  \hspace{1cm} (2.21)

where $\alpha$ is the coupling ratio caused by parasitics, $V_{dd}$ is the clock amplitude. Under such condition, $M$ is fully turned on to guarantee a complete charge transfer from $n_1$ to $n_2$. Unlike the Dickson charge pump, the potential of $n_1$ and $n_2$ can reach the same at the end. And it corresponds to the charge transfer stage.

In $S_4$, $\varphi_2$ becomes high again to turn $M_g$ on, making $M$ diode connected again to prevent charge flow-back.

The result of the threshold voltage cancellation is a higher pump gain:

$$\Delta V_{N4P} = \frac{CV_{dd}}{C + C_s} - \frac{I_{out}}{(C + C_s)f},$$ \hspace{1cm} (2.22)

Comparing Eq.2.18 and Eq.2.22, the pump gain of N4P is not degraded by the threshold voltage. And the output of a N4P can be expressed in Eq.2.23, which is higher than Eq.2.17 of the Dickson charge pump by a significant amount.

$$V_{out} = V_{dd} - V_{th}(N + 1) + N(\Delta V_{N4P}),$$ \hspace{1cm} (2.23)

where $V_{th}(N + 1)$ is the threshold voltage for the output stage of N4P.

### 2.4.2 Limits in the conventional N4P

While the N4P charge pump has higher output voltage, there are still some problems within the structure.

The most well-known one is the over-stress problem. Because all the bodies of NMOS are connected to the ground, the oxide layer of NMOS in the latter stages bears large stress. The oxide endurance of today’s standard MOS transistors is usually around 10V (10MV/cm on 10nm oxide). Higher voltage across the oxide brings the Fowler-Nordheim Tunneling effect [5]. The tunneling current density is given by [5] in Eq.2.24, where $\alpha'$ and $E_c$ are constant, $V_{tox}$ is the voltage across the oxide.

$$J = \alpha' \left( \frac{V_{tox}}{V_{tox}} \right)^2 e^{-\frac{V_{tox} E_c}{V_{tox}}}.$$ \hspace{1cm} (2.24)
2. CHARGE PUMP ANALYSIS AND TYPICAL STRUCTURES

This tunneling current damages the transistors dramatically with the rise of oxide voltage. As a result, high voltage transistors must be used, and this leads to higher cost and more parasitics.

Another problem is the gain degradation. Despite of the threshold voltage cancellation in N4P, the body effect expressed in Eq.2.19 still remains. As explained in Section 2.1, Eq.2.21 holds in S3 to cancel the threshold voltage. However, there is an assumption behind this. To turn on transistor $M$, the following relation should be satisfied

$$V_{ng} - V_{n2} = V_{n1} + \alpha V_{dd} - V_{n2} > V_{th(n)}, \quad (2.25)$$

and to finish the complete charge transfer, namely $n1$ and $n2$ finally reach the same potential, the following relation should also hold when charge transfer is over.

$$V_{ng} - V_{n2} = V_{n1} + \alpha V_{dd} - V_{n1} = \alpha V_{dd} > V_{th(n)}. \quad (2.26)$$

If Eq.2.26 is not satisfied, gain degradation occurs, while if Eq.2.25 is not satisfied, threshold voltage cancellation does not happen.

Combining Eq.2.19, Eq.2.22 and Eq.2.26, and taking $\alpha = 1, C_s = 0, I_{load} = 0$ for simplification, we can estimate the N4P’s maximum stages $N_{max}$ without degradation when:

$$V_{dd} = V_{th0} + \gamma \left( \sqrt{2\Phi_F} + (1 + N_{max}) V_{dd} - \sqrt{2\Phi_F} \right), \quad (2.27)$$

$$N_{max} = \frac{\left( \frac{V_{dd} - V_{th0}}{\gamma} + \sqrt{2\Phi_F} \right)^2 - 2\Phi_F}{V_{dd}} - 1. \quad (2.28)$$

Notice that $N_{max}$ also limits the N4P’s maximum output, and taking the output stage diode loss expressed in Equ.2.23 into consideration

$$V_{out, max} = (1 + N_{max}) V_{dd}. \quad (2.29)$$

From Eq.2.28 and Eq.2.29, the performance of N4P is severely degraded as the supply voltage goes down. And it is difficult for N4P to operate in lower than 2V supply.
2.4 NMOS Four Phase (N4P) Charge Pump

Even if Eq. 2.25 and Eq. 2.26 are satisfied. The rising threshold will limit the operation speed and the output current. The charge transferred in one period is

\[
Q = \beta \int \frac{1}{f} \left[ (V_{gs} - V_{th}(n)) V_{ds} - \frac{1}{2} V_{ds}^2 \right] d\left(\frac{1}{f}\right),
\]

where \( \beta = \mu C_{ox}(W/L) \), \( V_{gs} \) and \( V_{ds} \) are gate-source and drain-source voltage for a transistor. With the charge transferring, \( V_{ds} \) and \( V_{gs} \) become smaller and smaller. If \( V_{th}(n) \) is large, the charge transfer ability is largely restricted. And lower operation frequency \( f \) is needed to compensate. This also translate to larger capacitance, because \( I = CVf \). If a constant \( I \) and \( V \) is to be hold, lower \( f \) means larger \( C \).

Furthermore, as shown in Eq. 2.23, the threshold voltage of the output stage is also a large loss, since it bears the largest source-body bias. That is also one reason that many engineers choose the voltage doubler structure \([8, 12, 14]\) than the Dickson type, because this problem does not exist in the voltage doubler.
2. CHARGE PUMP ANALYSIS AND TYPICAL STRUCTURES
3

Charge Pump Circuit with Improved Charge Transfer Unit

In the previous chapter, the mathematical model of the charge pump circuit has been studied. The threshold and body effect problems of conventional charge pump structures are shown. In this chapter, we emphasis on how to design a better charge transfer unit to solve the problem at low cost.

3.1 Charge Pump Circuit Technology Review

Fig. 3.1-a shows the charge transfer unit of Dickson charge pump [1]. Clk and clkb are two out-of-phase clocks with amplitude equaling to the supply voltage $V_{dd}$. Ideally, an $N$ stage positive charge pump is capable to generate $+\left(N+1\right)V_{dd}$.

![Figure 3.1:](image)

Figure 3.1: a) Dickson charge pump[1], b) cross body connection scheme[2], c) four phase scheme[3], d) previous switched polarity charge pump[4].
output, and the $N + 1$ stage negative one is capable to generate $-(N + 1)V_{dd}$. However, due to the threshold voltage, body effect as well as the parasitics, the output of Dickson charge pump is largely limited [15].

Fig.3.1-b shows the cross body connection scheme [2]. It utilizes two auxiliary PMOS to control the body potential of the charge transfer PMOS transistor, in that way the threshold voltage is not rising with stages.

In paper [3], the four phase scheme is introduced, as shown in Fig.3.1-c. Notice that clk4 is not shown in the figure and is connected to the next stage. With this structure, the gate potential of the charge transfer transistor can be raise to a higher level than the drain potential, making the transistor fully open to let the potential between drain and source reach the same. Thus, this scheme is also called the threshold voltage cancellation scheme. The negative four phase charge pump using PMOS operates in the similar way. However, due to the fixed body potential (GND), it suffers from threshold rising problem as well. Over-stress is another problem.

As the limits of charge pump mainly result from the body effect and the threshold voltage loss, many recent developed high efficiency charge pumps [8, 10, 12] combine the techniques shown in Fig.3.1-b and c, namely PMOS cross body control and four phase. Although using PMOS to realize the body control is compatible to standard process, it may cause great problem in the switch polarity charge pump, which is discussed in Section 3.4.

Fig.3.1-d shows one stage of a previously published switch polarity charge pump [4]. The connection of the body, drain and gate result in a simple body-source junction diode, of which the threshold is much lower than a normal NMOS transistor, besides the threshold is not rising with stages and there is no over-stress. By this configuration, the stage can be shared in both positive and negative operation. However, even if the junction threshold is low, when the stage number is large in the low voltage supply, the loss is also significant.
3.2 Switched Polarity Charge Pump Architecture

Charge pump circuits play a very important role in the modern electronic systems [3, 14, 16, 17]. While most of the applications utilize only single polarity charge pump, in some cases, however, both positive and negative high voltage are required. Some kind of the flash memory, for example, use positive high voltage to program and negative high voltage to erase, which is shown in Fig. 1.1.

Traditionally, two set of charge pumps are implemented on the chip, one positive and one negative, but they do not function at the same time due to the different timing of the program and erase operation. This causes a tremendous waste of the chip area and power, since the total capacitance of a charge pump may exceed several tens of pico farad (pF) according to the supply voltage and the current requirement. In such systems, a switch polarity charge pump may be implemented to save the cost.

The architecture of proposed 5-stage four phase switched polarity charge pump is shown in Fig. 3.2. Except of the last p-stage, all others are n-stages using triple well technology. n-stage #1 is the additional stage needed by the negative operation for a lack of $-V_{dd}$ supply. High voltage transistor Mc0 ∼ Mc4 are responsible for the positive/negative switching operation according to the switch signal.

Figure 3.2: Architecture of proposed 5 stage switched polarity charge pump.
3. CHARGE PUMP CIRCUIT WITH IMPROVED CHARGE TRANSFER UNIT

![Figure 3.3: The proposed n-stage(left), p-stage(middle) and clock scheme(right).](image)

The configuration is similar to [4]. When ‘switch’ signal is low (GND), Mc0 is turned on and Mc2 is turned off, the charge begin to be transferred from $V_{dd}$ to $V_{out}$. This forms the positive charge pump. Consequently, Mc1 is turned on while Mc3 and Mc4 are turned off. On the contrary, when switch is high ($V_{dd}$), Mc0 and Mc1 are turned off while Mc2, Mc3 and Mc4 are turned on. This corresponds to negative charge pump.

### 3.2.1 Proposed N-stage Charge Transfer Unit

The proposed n-stage charge transfer unit and the clock scheme are shown in Fig.3.3. M1, M2 and Mb are all NMOS transistors. M1, M2 and the capacitor $C_g$ form the threshold cancellation scheme presented in Fig.2.4-c. The difference is that the body of M1 and M2 are connected to an auxiliary transistor Mb.

One clock period can be divided into four steps: $S_1$, $S_2$, $S_3$ and $S_4$ according to Fig.3.3(right). And the operation of n-stage for one clock period is listed in Table I.

Charge transfer takes place in $S_3$ when M1 is turned on and the potential of $ng$ is boosted to a higher level. Notice that Mb is also turned on in this period, which shorts $nb$ and $nh$. The relation among $nl$, $nh$ and $nb$ is expressed in Eq.3.1

$$V_{nb} = V_{nh} \leq V_{nl}. \quad (3.1)$$

On the other hand, when Mb, M1 is turned off and M2 is turned on in $S_1$, $S_2$ and $S_4$. Mb’s potential is mainly determined by the the capacitance model...
of M1 and Mb, which can be express in Eq.3.2.

\[ V_{nb} = \frac{C_{SB} + C_{DBb}}{C_t} V_{nh} + \frac{C_{DB}}{C_t} V_{nl} + \frac{C_{GB} + C_{GBb}}{C_t} V_{ng}, \]  

(3.2)

where \( C_{GB}, C_{DB} \) and \( C_{SB} \) are M1’s gate-body, drain-body and source-body capacitance respectively, while \( C_{GBb} \) and \( C_{DBb} \) are Mb’s gate-body and drain-body capacitance respectively. Because Mb’s source and body is connected, its source-body capacitance is ignored. And \( C_t = C_{GB} + C_{DB} + C_{SB} + C_{GBb} + C_{DBb} + C_s \), \( C_s \) is the parasitics including the M1 and Mb’s substrate capacitance. From Table I, we also know \( V_{nh} > V_{nl} = V_{ng} \) in S1, S2 and S3, and consider \( C_{SB} + C_{DBb} \) is negligible compared to \( C_t \), then we can approximate Eq.3.2 into Eq.3.3.

\[ V_{nb} = \frac{C_{DB} + C_{GB} + C_{GBb}}{C_{GB} + C_{DB} + C_{SB} + C_{GBb} + C_{DBb} + C_s} V_{nl}. \]  

(3.3)

Let \( \beta = \frac{C_{SB} + C_{DBb} + C_s}{C_{GB} + C_{DB} + C_{GBb}} \), we get \( V_{nb} \) in Eq.3.4.

\[ V_{nb} = \frac{1}{1 + \beta} V_{nl}. \]  

(3.4)

Basically, \( C_{GB} \) is much larger than \( C_{SB}, C_{DBb} \) or \( C_s \). As a result, we can make \( \beta \ll 1 \) by choosing a moderate size for Mb, 10% of the M1’s size is acceptable. And the relation among \( nl, nh \) and \( nb \) in S1, S2 and S3 are expressed in Eq.3.5.

\[ V_{nb} \approx V_{nl} < V_{nh}. \]  

(3.5)

From Eq.3.1 and Eq.3.5, we can conclude that \( nb \)'s potential follows closely to the lower one between \( nl \) and \( nh \), which makes sure that the body-drain and

<table>
<thead>
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<th>step</th>
<th>clk1</th>
<th>clk2</th>
<th>clk3</th>
<th>M1</th>
<th>M2</th>
<th>Mb</th>
<th>potential</th>
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<tbody>
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<td>L</td>
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<td>L</td>
<td>off</td>
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<tr>
<td>S2</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>off</td>
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<td>S3</td>
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<tr>
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<td>L</td>
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<td>( V_{nh} &gt; V_{nl} = V_{ng} )</td>
</tr>
</tbody>
</table>

Table 3.1: Operation of the n-stage in one clock period
the body-source PN junction is not turned on and suppress the junction leakage current. Moreover, when M1 is turned on in $S3$, the M1’s body and source is short, which prevents M1 from body effect.

We do not directly implement the cross body scheme shown in Fig.2.4-b, because when the potential of $nl$ and $nh$ come close, the two auxiliary transistor shown in Fig.2.4-b can not be turned on. And this scheme is also susceptible to the risk of latch up [18].

### 3.2.2 Proposed P-stage Charge Transfer Unit

Fig.3.3(middle) shows the PMOS counterpart of the n-stage. It works as the output stage when the proposed charge pump, shown in Fig.3.2, is positive, while input stage when negative, because the $nh$’s potential of the n-stage is used to control M2 and can not be fixed. By a substitute of the p-stage, we avoid of using a diode connected transistor [1, 3, 10], which causes voltage loss.

### 3.3 Simulation Results and Comparison

The simulations are executed on the 0.13µm technology. For the n-stage, $C_g=50fF$, M1’s W/L=50, the size of M2 and Mb are 10% of M1. Transistors in p-stage are two times those of n-stage correspondingly, main capacitor C=5pF, and load capacitor CL=10pF. The clock frequency $f$ is 10MHz and supply voltage $V_{dd}$ is 1.5V. To compare the performance, simulations on [3, 4] with the same parameters are also performed.

The unloaded output transient chart for the proposed 5 stage switch polarity charge pump is shown in Fig.3.4. The output of the proposed charge pump achieves $+8.87V/-8.84V$, 98% of the ideal $+9V/-9V$ output. And the set up time is about $10\mu s$. With 10% of total capacitance (0.5pF each stage) as estimated parasitics, the output is $+8.22V/-8.05V$, 90% of the ideal output.

In Fig.3.5, the output voltage with different stages is shown. As the number of stage increase, the proposed charge pump shows good linearity, while the output of [3] becomes saturate due to the threshold rising problem. [4] also shows good linearity but the voltage loss is significant. Fig.3.6 compares the output under
3.3 Simulation Results and Comparison

Figure 3.4: Unloaded output transient (comparison with Mohammad[4], Lin[3], 5 stages, $V_{dd} = 1.5$V).

Figure 3.5: Output voltage vs. number of stages (comparison with Mohammad[4], Lin[3], $V_{dd} = 1.5$V).
3. CHARGE PUMP CIRCUIT WITH IMPROVED CHARGE TRANSFER UNIT

Figure 3.6: Output voltage vs. supply voltage (comparison with Mohammad[4], Lin[3], 5 stages).

Figure 3.7: Output characteristics for the proposed 5-stage charge pump.
3.4 Reliability Issue

![Diagram](image)

**Figure 3.8:** a) Forward biased PN junction b) Triple well control.

different supply conditions. Owning to the threshold cancellation and body control scheme, the output of proposed switch polarity charge pump follows the ideal value closely, even under 10% parasitics condition.

Fig.3.7 shows the current output characteristics of proposed 5-stage switched polarity charge pump. The slope \(-\Delta V/\Delta I\) which indicates the equivalent inner resistance is about 0.10MΩ for positive output and 0.12MΩ for negative output.

### 3.4 Reliability Issue

In this section, we discuss about reliability issue which may occur in the real chip implementation.

In switched polarity charge pump, body control and NMOS triple well is essential. If the body is fixed to GND, the body-drain and body-source PN junction of NMOS can be turned on when the charge pump is negative, and so are those of PMOS when positive, which is shown in Fig.3.8-a. With body control scheme, the body potential is able to follow the source or drain. However, PMOS body control which is compatible to standard process may also cause trouble. Due to the fixed GND of the P-substrate, substrate current occurs when the N-type body goes negative in the charge pump’s negative operation.

As a result, triple well NMOS transistors as well as deep N-well potential control scheme, shown in Fig.3.8-b, should be implemented. When the charge pump is positive, which means the switch is low, the P-type body and deep N-well
3. CHARGE PUMP CIRCUIT WITH IMPROVED CHARGE TRANSFER UNIT

are connected. The PN junction between substrate and N-well is reverse biased in this situation. On the other hand, when the charge pump is negative, which means the switch is high, the N-well is connected to GND. This makes the PN junction between P-type body and N-well reverse biased. By this configuration, the substrate current is prevented.

For the p-stage in the proposed charge pump, when the charge pump is negative, the N-type body should be connected to GND and the body control scheme should be break. Since the p-stage is input stage in negative operation and suffers from the least body effect, this causes little impact on the performance.

Although additional control circuit may bring more parasitics, the advantages of switch polarity charge pump is overwhelming. We have also performed simulations under 10% estimated parasitics to examine the impact, which is shown in Fig.3.4, Fig.3.5, Fig.3.6 and Fig.3.7.

3.5 Conclusion

In this Chapter, a four phase switched polarity charge pump is presented. Four phase threshold voltage cancellation and body control scheme are implemented to achieve high performance. The output of the proposed charge pump is able achieve 90% of the ideal value even under 10% of estimated parasitics, and shows good linearity with increase of stages. Reliability issue is also discussed to prove the validity.
4

High Efficiency Charge Pump Circuit with Charge Sharing Clock Scheme

4.1 Double Charge Sharing Clock Scheme

In this section, the charge pump efficiency is discussed, and a dual charge pump circuit with complementary architecture using charge sharing clock scheme is presented. The proposed charge sharing clock generator is able to recover the charge from parasitic-capacitor charging and discharging, so that the dynamic power loss in the pumping process is reduced by a half. To preserve the overlapping period of the four-phase clock used for threshold cancellation technique, two complementary sets of clocks are generated from the proposed clock generator, and each set feeds a certain branch of the dual charge pump to achieve the between-branch charge sharing. A test chip is fabricated in 0.18μm process, and the area penalty of the proposed charge sharing clock generator is 1%. From the measurement results, the proposed charge pump shows an overall power efficiency increase with a peak value of 63.7% comparing to 52.3% of a conventional single charge pump without charge sharing, and the proposed clock scheme shows no degradation on the driving capability while the output ripple voltage is reduced by 43%.
4. HIGH EFFICIENCY CHARGE PUMP CIRCUIT WITH CHARGE SHARING CLOCK SCHEME

![Charge Pump Circuit Diagram](image)

Figure 4.1: N-stage charge pump model.

4.1.1 Introduction

The charge pump circuits are used to generate a higher voltage from the power source. Owing to the capacitor-only design and relatively compact size, they have been widely adopted in various kinds of non-volatile memories (NVM) to provide the programming or erasing high voltage \([17, 19, 20]\). These years, due to the growing demand of longer battery life for portable applications such as PDAs, mobile phones and tablet PCs, low power consumption has become one of the main concerns in the NVM design \([20, 21, 22]\). Following this trend, the charge pump circuits, as one of the main power consumers in NVMs, have gathered more attention on the power efficiency performance \([2, 3, 7, 8, 9, 23, 24, 25, 26]\).

Shown in Fig.4.1 is a canonical N-stage charge pump model, in which each stage is composed of a series connected switch \(S_n\) and a capacitor \(C\). The \(C_p\) is the bottom plate parasitic capacitor of \(C\) with a parasitic ratio \(\alpha\). Switches are used to prevent the current from flowing back, and the capacitors are for the charge storage. With two out-of-phase clocks respectively driving the bottom plate of the odd and even stage capacitors, the charge is able to accumulate on the load capacitor creating a potential several times higher than \(V_{dd}\). Fundamentally, expect for the equivalent inner resistance which is a function of stage number, capacitance size and the frequency \([27]\), the power loss of an on-chip charge pump circuit comes from three aspects:

- The switch loss due to the incomplete charge transfer and reverse leakage of each switch \(S_n\).
4.1 Double Charge Sharing Clock Scheme

- The coupling loss caused by insufficient gate boosting due to the parasitic capacitance of each node 1 to \( n \).

- The dynamic loss due to charging and discharging the bottom plate parasitic capacitor \( C_p \).

Many works have been published to improve the power efficiency of the charge pump circuits, while most of them have focused on eliminating the switch loss, among which the four-phase clock threshold cancellation and the body effect cancellation techniques are the most effective and popular \([2, 3, 7, 8]\). The coupling loss is related to the switch circuit structure and technology. With a more efficient switch implementation and faster transistors, the switch size can be smaller so as the parasitic capacitance at each node \([26]\). Beside the above two aspects, Palumbo et al. has pointed out that the most dominant factor to the charge pump power efficiency comes from the dynamic loss, and the efficiency boundary with only bottom plate parasitic considered is concluded in the following equation \([25]\):

\[
\eta = \frac{K}{N + 1 + \alpha \frac{N^2}{N+1-K}},
\]

where \( N \) is the stage number, \( \alpha \) is the bottom plate parasitic ratio and \( K = V_{out}/V_{dd} \). The efficiency plot is shown in Fig.4.2. Generally, the choice of metal-insulator-metal capacitor yields a smaller \( \alpha \), but the area consumption is quite large. Instead, gate capacitor with larger \( \alpha \) around 0.1 to 0.2 is usually adopted to reduce the cost while sacrificing the power efficiency. To compensate this drawback, the charge sharing concept proposed in \([23]\) is able to recover half of the charge from parasitic-capacitor charging and discharging. However, since the sharing is based on two overlapping clocks, the overlapping period is destructed, which increase the switch on-resistance and cause an incomplete charge transfer for heavy load or low voltage supply condition. Besides, since the charge sharing is conducted between stages, an even stage number of the charge pump is also necessary to equalize the parasitics on each clock driver. Another charge sharing implementation is reported in a cross-coupled charge pump \([24]\), while additional care must be taken to prevent the leakage current including the use of a local
4. HIGH EFFICIENCY CHARGE PUMP CIRCUIT WITH CHARGE SHARING CLOCK SCHEME

![Graph showing charge pump efficiency with only bottom plate parasitic considered.]

**Figure 4.2:** N-stage charge pump efficiency with only bottom plate parasitic considered.

level shifter every stage, which increase the circuit complexity introducing more parasitics and more additional power consumption.

To solve these problems, a new dual charge pump circuit with complementary architecture using charge sharing clock scheme is proposed in this paper. The proposed charge pump consists of two complementary branches, and two complementary sets of clocks are generated from the proposed charge sharing clock generators to feed each branch. Four-phase clock threshold cancellation and body-effect cancellation techniques are also implemented to eliminate the switches loss. Instead of between-stage charge sharing, the proposed charge sharing clock scheme is based on between-branch charge sharing, in which way the overlapping high or low period of each set of four-phase clock is completely preserved, and the number of stage is not limited to even. A test chip of a proposed dual charge pump and a conventional charge pump are fabricated in 0.18µm technology, and the measurements are conducted under 1V, 1.2V and 1.5V supply condition. The results show that more than 10% increase in the peak power efficiency is achieved with no driving capability decline in each case, while the ripple voltage is reduced by nearly a half comparing to the conventional charge pump.
4.1 Double Charge Sharing Clock Scheme

4.1.2 The Charge Sharing Concept and Efficiency Analysis

The charge sharing concept and its waveform are shown in Fig. 4.3, where $C_1$ and $C_2$ are two capacitors of the same size loading two out-of-phase clocks, Clk1 and Clk2.

Initially, $C_1$ is charged to $V_{dd}$ and $C_2$ is discharged to ground. Before discharging $C_1$ to ground and charging $C_2$ to $V_{dd}$, a connection between $C_1$ and $C_2$ is temporarily enabled until each of their potential is equalized to $V_{dd}/2$. In this way, only the charging from $V_{dd}/2$ to $V_{dd}$ for $C_2$ is required from the supply. In the next clock change before discharging $C_2$ to ground, the same operation is repeated, which is also indicated in Fig. 4.3. If $C_1$ and $C_2$ are treated as the parasitics that $C_1 = C_2 = \alpha C$, and the clock runs at a frequency of $f$, the power consumption for charging each capacitor from the supply is obtained as:

$$P_s = f \cdot \int_{\frac{1}{2} \alpha CV_{dd}}^{\alpha CV_{dd}} V_{dd} \cdot dQ = \frac{1}{2} \alpha C f V_{dd}^2,$$

(4.2)

however, suppose that Clk1 and Clk2 run independently without charge sharing,
the power consumption for charging each capacitor is:

\[ P = f \cdot \int_{0}^{\alpha C V_{dd}} V_{dd} \cdot dQ = \alpha C f V_{dd}^2. \]  

(4.3)

Comparing equation (4.3) with (4.2), it is clear that the power consumption of the charge sharing clock is reduced by a half. On the other hand from the mathematical expressions, it can also be translated to that the equivalent parasitic ratio of the charge sharing clock has been reduced to \( \alpha/2 \). Therefore, the efficiency boundary of a charge pump with charge sharing clocks becomes:

\[ \eta_s = \frac{K}{N + 1 + \frac{\alpha}{2} \frac{N^2}{N+1-K}}. \]  

(4.4)

For a conventional charge pump with parasitic ratio \( \alpha = 0.1 \), the efficiency boundary is as the dash line shown in Fig.4.2. Provided the charge sharing clock is adopted, the efficiency boundary becomes that of \( \alpha = 0.05 \), the solid line in Fig.4.2.

It should be noticed that the charge sharing clocks always occur in pair which are out-of-phase to each other, and the charge sharing concept is more useful for the situation with higher parasitic ratio, since more dynamic loss is to be recovered.

4.1.3 The Proposed Charge Sharing Clock Generator and The Dual Charge Pump Circuit

4.1.3.1 Charge Sharing Clock Generator Unit

According to the charge sharing concept shown in Fig.4.3, the proposed charge sharing clock generator is shown in Fig.4.4, where \( C_p \) represents the parasitic capacitors of the charge pump driven by two clock drivers, and the delay unit is constructed by the inverter chain.

The charge sharing operation is controlled by two switches \( S1, S2 \), and a NMOS transistor \( N1 \). The control signal \( ctrl \) is the exclusive-or (XOR) result of \( clk_{in} \) and its delayed signal \( clk_{d} \). During \( ctrl \) is high before the drivers’ outputs change, \( S1 \) and \( S2 \) are turned off to isolate each \( C_p \) from the drivers, and \( N1 \) is turned on to enable charge sharing between those two \( C_p \). After the
4.1 Double Charge Sharing Clock Scheme

Figure 4.4: The proposed charge sharing clock generator.

Figure 4.5: Simulation result of the charge sharing clock.
4. HIGH EFFICIENCY CHARGE PUMP CIRCUIT WITH CHARGE SHARING CLOCK SCHEME

charge sharing is complete, the drivers’ outputs must change before \( \text{ctrl} \) goes low, because if \( S1 \) and \( S2 \) are turned on before the change, the potential on each \( C_p \) returns to the initial value resulting in the operation failure, while this timing is easily guaranteed by a longer delay in XOR than the driver. When \( \text{ctrl} \) goes low, \( S1, S2 \) are turned on and \( N1 \) is turned off, and the rest charging and discharging for \( C_p \) is complete by the supply and ground. The operation in the next clock change is the same. For a certain capacitor size, the delay time between \( \text{clk}_{in} \) and \( \text{clk}_d \) is determined by the \( N1 \)’s size. A large size indicates a large current which means less time is required to complete the charge sharing, whereas it also means that more dynamic power on the transistor is to be cost. As a result, a balance should be made between delay time (speed) and local power consumption.

The simulation result of the charge sharing clock generator is shown in Fig. 4.5, where the \( C_p \) is 10pF for test and \( V_{dd} \) is 1.2V. For the ordinary clock, the supply starts to charge as soon as the clock changes, while for the charge sharing clock, the charge starts after the sharing process is finished. The peak current of the charge sharing clock is reduced to nearly one third and average consumption is nearly a half.

4.1.3.2 Dual Charge Pump Circuit with Complementary Architecture

As mentioned before, four phase overlapping clocks are often utilized to improve the charge pump performance \([3, 23, 24]\). However, if the charge sharing is applied to a single charge pump, the overlapping period can not be ensured, which is illustrated in Fig.4.6. For original clocks, during the overlapping high period of \( \text{clk}1 \) and \( \text{clk}2 \), capacitor \( C_g \) is precharged through transistor \( N2 \) to the same level as node \( nl \), so that transistor \( N1 \)’s gate can be boosted to a much higher potential when \( \text{clk}3 \) goes high. If the charge sharing is introduced to the two clocks, the precharged potential on \( C_g \) becomes much lower, since the clock voltage is only half of the original value during the overlapping period. For low voltage operation, transistor \( N2 \) might not even be turned on. In order to overcome the problem, a dual charge pump with complementary architecture using two complementary sets of overlapping clocks is proposed, which is shown in Fig.4.7
4.1 Double Charge Sharing Clock Scheme

The proposed dual charge pump circuit is constructed by two complementary branches with equal stage capacitance, and they work in a complementary manner. Since the clock signals of the two branches are complementary in nature, the overlapping period between stages can then be preserved by only introducing the charge sharing to the corresponding clocks between branches. It should be notice that, without a complementary architecture, the problem shown in Fig. 4.6 remains because only the clock arrangement is changed for the two branches of conventional dual charge pump circuit [28].

The lower branch of the proposed double charge pump is mainly composed by NMOS stages, $N_{stg}$. The charge transfer transistor $N1$ and the auxiliary transistor $N2$ together with a small charge blocking capacitor $C_g$, usually around 1% of $C$, fulfill the threshold cancellation in the same manner as the conventional NMOS four phase charge pump circuit [3]. Transistor $Nb$ is used to track the body of $N1$ to a lower potential. When $N1$ is turned on to transfer charge from node $nl$ to $nh$ ($V_{nl} \geq V_{nh}$), $Nb$ is also turned on so that $N1$’s body is short to $nh$, and the body effect of $N1$ is eliminated during this period. When $N1$ is turned off in the charge block period, $Nb$ is turned off as well so that the body-source or body-drain PN junction of $N1$ is not turned on. Since the body potential of NMOS transistors is controlled, the $N_{stg}$ should be realized in triple well technology. The upper branch of the proposed double charge pump is mainly composed by PMOS stages, $P_{stg}$. The $P_{stg}$ is complementary to the $N_{stg}$, and the operation of upper branch is also complementary to the lower one. The

**Figure 4.6:** Charge sharing on single charge pump destructs the overlapping period.
4. HIGH EFFICIENCY CHARGE PUMP CIRCUIT WITH CHARGE SHARING CLOCK SCHEME

![Diagram of a high efficiency charge pump circuit with charge sharing clock scheme]

**Figure 4.7:** Proposed 5 stage dual charge pump with complementary architecture.
4.1 Double Charge Sharing Clock Scheme

Figure 4.8: The N-set and P-set clocks generation.

\( P_{stg} \) in lower branch is used to eliminate the output loss because \( N_{stg} \) would malfunction if the potential of node \( nh \) is fixed. Similarly, a \( N_{stg} \) is used as the input stage of the upper branch.

The \( N\)-set clock with overlapping-high period between \( clk1 \) and \( clk2 \) is used to feed the lower NMOS branch, while the \( P\)-set clock with overlapping-low period between \( clk1' \) and \( clk2' \) is used to feed the upper PMOS branch. The \( clk1 \) and \( clk1' \), \( clk2 \) and \( clk2' \) are two pairs of complementary clocks produced by the charge sharing clock generator shown in Fig.4.4 respectively. The \( clk3 \) and \( clk3' \), \( clk4 \) and \( clk4' \) are also complementary, however, since capacitor \( C_g \) is very small comparing to \( C \), usually around 1\%, the parasitics of \( C_g \) is negligible and charge sharing is unnecessary. The \( N\)-set and \( P\)-set clocks generation circuit and the clock connections are shown in Fig.4.8.

Owning to the complementary architecture, the overlapping period of each clock set, which is essential for the charge pump to work properly at low voltage,
4. HIGH EFFICIENCY CHARGE PUMP CIRCUIT WITH CHARGE SHARING CLOCK SCHEME

Figure 4.9: Chip die photograph of the proposed 5-stage dual charge pump circuit (880µm x 280µm).

is able to be preserved. Thus, the driving capability is guaranteed. Besides, since the charge sharing operation happens between two branches, the stage number is not necessary to be even. Moreover, the implementation of the dual charge pump architecture yields a substantial decrease in the output ripple voltage [28].

4.1.4 Results and Discussion

In order to prove the validity, the proposed 5-stage dual charge pump circuit with charge sharing clock scheme is fabricated in 0.18µm CMOS process with triple-well technology, and the main design parameters are summarized in Table I.

The chip die photograph is shown in Fig.4.9. Capacitors are M-I-M type

<table>
<thead>
<tr>
<th>Table 4.1: Main Design Parameters.</th>
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<tbody>
<tr>
<td>Technology</td>
</tr>
<tr>
<td>Stage number $N$</td>
</tr>
<tr>
<td>Supply voltage $V_{dd}$</td>
</tr>
<tr>
<td>Clock frequency $f$</td>
</tr>
<tr>
<td>Boost capacitance $C_g$</td>
</tr>
<tr>
<td>Pumping capacitance $C$</td>
</tr>
<tr>
<td>Load capacitance $C_L$</td>
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</tbody>
</table>
4.1 Double Charge Sharing Clock Scheme

with bottom-plate parasitic ratio around 0.1. The area consumption of the whole circuit is $0.2464 \, mm^2$ ($880 \mu m \times 280 \mu m$). Since the body terminals in each $N$-stg as well as $P$-stg are connected together, all the transistors in each stage is arranged in the same P or N well to save area cost. To have an equal on-resistance, the W/L ratios in $P$-stg are 2.5 times those in $N$-stg respectively. Since the $N$-stg is constructed in triple well, the actual size of $P$-stg and $N$-stg on the chip looks the same. Two proposed charge sharing clock generators are implemented to the dual charge pump while the area occupation is less than 1%. For comparison reason, a conventional 5-stage four-phase single branch charge pump circuit is also implemented on the chip. The circuit design is the same as the PMOS upper branch shown in Fig.4.7, while all the size is doubled to achieve the same parameters.

Shown in Fig.4.10 is the measurement result of the proposed charge sharing clock generator. The supply voltage is 1.2V and the clock frequency is 1MHz. It can be confirmed that the charge sharing operation is finished at approximate 0.6V, half of the supply, indicating nearly a half reduction of the dynamic consumption is achieved. Fig.4.11 shows the measured output voltage at 1MΩ load, where channel 1 is the waveform of the conventional charge pump, and channel 2 is the waveform of the proposed double charge pump. Although both of the average output voltage is able to reach 5.59V, however, owning to the double branch architecture which is able to deliver the charge to output more smoothly, the ripple voltage of the proposed charge pump is only 46.9mV comparing to the 81.9mV of the conventional charge pump.

To better evaluate the proposed dual charge pump circuit with charge sharing clock scheme, further measurements on I-V characteristic, output ripple voltage and power efficiency are conducted under the conditions of 1V, 1.2V and 1.5V supply respectively. The performance on the switch loss, the coupling loss and the dynamic loss, which have been introduced in section I, is also to be discussed in the following.

For all the applications, the first concern of the charge pump design is the driving capability, or the effectiveness of charge delivery. It is usually evaluated by the V-I curves, and is strongly related to the switch loss as well as the coupling loss. A good driving capability leads to fewer charge pump stages and smaller
4. HIGH EFFICIENCY CHARGE PUMP CIRCUIT WITH CHARGE SHARING CLOCK SCHEME

Figure 4.10: Measurement result of charge sharing clock generator \((V_{dd}=1.2\, \text{V}, f=1\, \text{MHz})\).

Figure 4.11: Measurement results of the charge pump output voltage \((V_{dd}=1.2\, \text{V} \text{ at } 1\, \text{M\Omega load, CH1: the conventional CP, CH2: the proposed CP)}\).

area, while a poor driving capability may result in the incomplete charge transfer for heavy load conditions. The V-I characteristic of the proposed charge pump is shown in Fig.4.12-a), where the round marks represent the measurement data of the proposed charge pump, the square marks represent the data of the conventional charge pump, and the solid lines are their fitting curves. The V-I curves of the proposed charge pump follow closely to that of the conventional one, while the output voltage becomes a little higher in heavy load conditions. This result suggests that the four-phase threshold cancellation scheme works normally for the proposed charge sharing clock scheme, and the driving capability has not de-
4.1 Double Charge Sharing Clock Scheme

Figure 4.12: a) measured output voltage. b) measured ripple voltage.
4. HIGH EFFICIENCY CHARGE PUMP CIRCUIT WITH
CHARGE SHARING CLOCK SCHEME

coupled even in 1V supply. The stage coupling loss comes from the total parasitic
 capacitance at the top node of each stage capacitor, that only a part of $V_{dd}$ is
coupled on the top plate when the clock rises at the bottom plate, and it affects
the charge pump output by a coupling ratio $\beta$ at each stage, which is expressed
as [1]:

$$V_{out} = \beta(N + 1)V_{dd} - \frac{NI_L}{fC},$$  \hspace{1cm} (4.5)

where $I_L$ is the output current. The coupling ratio can then be obtained through
the free load output voltage ($I_L = 0$), namely, the cross point between I-V curve
and the x-axis:

$$\beta = \frac{V_{out}}{(N + 1)V_{dd}},$$  \hspace{1cm} (4.6)

which is about 0.96 for the proposed charge pump circuit while $\beta=1$ is the ideal
case. Since the switch loss is almost eliminated by the four phase threshold
cancellation and body effect cancellation scheme, it is not considered in eq.(4.5).

The ripple voltage is another important concern of the charge pump circuits,
especially for the non-volatile memory applications. A smaller ripple on the
output voltage contributes to a more precise programming or erasing operation
and low bit error rate, which is desirable for high data throughput and retention
[29, 30]. Conventional single branch charge pump has a ripple voltage of [27]:

$$V_r = \frac{\Delta Q}{C_L} = \frac{I_L}{fC_L},$$  \hspace{1cm} (4.7)

and the ripple reduction is usually based on increasing the size of decoupling
capacitance $C_L$. However, since the double branch architecture is utilized in the
proposed charge pump, the load is fed by each branch in a different half period
[28]. Therefore, the charge $\Delta Q$ pumped at the output is divided into two equal
parts for each half period, and thus the ripple voltage becomes:

$$V_r = \frac{\Delta Q}{2C_L} = \frac{I_L}{2fC_L},$$  \hspace{1cm} (4.8)

which is only a half comparing to the conventional single branch charge pump.
The ripple voltage of the proposed dual charge pump is shown in Fig.4.12-b), and
from calculating the slope of each fitting curve, about 43% of the ripple reduction
is achieved in all cases with the same size of decoupling capacitance.
4.1 Double Charge Sharing Clock Scheme

![Graph showing power efficiency with and without charge sharing clock](image)

**Figure 4.13:** Measured power efficiency ($\alpha = 0.1$).

The power efficiency of charge pump circuit is the key point for low power applications. Most of the previous works have successfully realized various kinds of ideal switches, which has no switch loss and less coupling effect, whereas little progress has been made on lowering the dynamic consumption. With the proposed clock scheme, a between-branch charge sharing is achieved so that the dynamic loss on the parasitics is able to be reduced by a half. The power efficiency $\eta$ is calculated by the following:

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}} + P_{\text{drv}} + P_{\text{csh}}},$$  

(4.9)

where $P_{\text{out}}$ is the output power, $P_{\text{in}}$ is the input power, $P_{\text{drv}}$ is the clock driving power and $P_{\text{csh}}$ is the consumption of the proposed charge sharing clock generator, which is not included in the calculation of the conventional charge pump. The efficiency comparison is shown in Fig.4.13, where the parasitic ratio is around 0.1.
4. HIGH EFFICIENCY CHARGE PUMP CIRCUIT WITH CHARGE SHARING CLOCK SCHEME

![Graph showing comparison between Proposed 14-stage CP and Conventional 14-stage CP](image)

**Figure 4.14:** Simulation result of the 14 stage proposed dual charge pump ($V_{dd}$=1.2V, $\alpha$=0.1, $N$=14, $I_L$=4$\mu$A).

For all the supply cases, the efficiency curves of the proposed and conventional charge pumps are well converged. This comes from the fact that the switch loss has nearly been eliminated while the couple loss is not relevant to the supply, and thus the power efficiency is dominated by the dynamic loss, which is explained by Eq.(4.1) and Eq.(4.4). The efficiency of 1.5V case is a little lower since the through current in clock driver becomes large for higher supply conditions. The peak power efficiency of the proposed charge pump is 63.7%, while it is 52.3% for the conventional one, and a peak efficiency increase of nearly 11% is achieved. The reason why measurement results are not in accordance with the calculated results shown in Fig.4.2 is mainly because the stage coupling ratio is assumed to be 1 in Eq.(4.1) and Eq.(4.4) but it is 0.96 for the test chip and the parasitic ratio is not exactly 0.1 as well (around 0.1 to 0.11). However, the effectiveness of the charge sharing clock scheme is well confirmed.
4.2 Triple Charge Sharing Clock Scheme

Since most of the commercial non-volatile memories require a program voltage between 10V ~ 20V, simulations are performed on a 14 stages proposed dual charge pump and a 14 stages conventional charge pump, and the other design parameters are the same as Table I. The results are shown in Fig. 4.14 for reference. Under 4µA load current, both of the charge pump achieve 15V output voltage. For the supply current, owing to the charge sharing operation, the peak parasitic charging current of the proposed charge pump is only about 0.64mA while it is 2.24mA for the conventional charge pump, and since double branch architecture is utilized, the stage charge transfer current is more smooth [28]. The power efficiency of the proposed charge pump under such condition is 60.9% comparing to 51.3% of the conventional one.

4.2 Triple Charge Sharing Clock Scheme

In this section, a dual charge pump circuit with triple charge sharing clock scheme is described. The proposed charge sharing clock generator is able to recover nearly two-thirds of the charge from the parasitics charging, in which way the dynamic power loss in the pumping process is reduced to almost one-third. To preserve the overlapping period of the four-phase clock the complementary charge pump architecture is used to achieve the between-branch charge sharing.

Under 0.18µm technology with a bottom plate parasitic ratio of 0.2, the simulation results of a proposed 5-stage charge pump circuit show an overall efficiency increase with a peak value of 62.8% comparing to 46.8% of a conventional one, and the output ripple voltage is reduced by nearly a half.

4.2.1 Introduction

As introduced previously, the theoretical efficiency boundary of such charge pump circuits is concluded as:

\[ \eta = \frac{K}{N + 1 + \alpha \frac{N^2}{N+1-R}}, \]

(4.10)

where \( K = V_{\text{out}}/V_{\text{dd}} \), \( N \) is the stage number, and all the switches are treated as ideal ones. For a certain number of stages \( N \), the efficiency boundary is dominant.
4. HIGH EFFICIENCY CHARGE PUMP CIRCUIT WITH CHARGE SHARING CLOCK SCHEME

by parasitic ratio $\alpha$. In order to break this limit, the charge sharing concept, or the dual-charge sharing, proposed in [23] is able to reduce the consumption by a half so that the equivalent bottom plate parasitic ratio becomes $\alpha/2$, and in a previous published paper [31], we have improved the low voltage performance by adopting the scheme to the double charge pump architecture that realize a between-branch charge sharing, and the stage number of the charge pump circuit needs not to be even which is a main constrain in the original scheme.

In this section, the charge sharing concept is extended to triple charge sharing which is able to recover nearly two-thirds of the energy from the parasitics charging, and the dynamic power loss of the charge pump circuit is reduced to almost one-third. Dual charge pump architecture is also utilized to achieve the between-branch sharing. Simulation on a proposed 5-stage double charge pump under 0.18$\mu$m technology with 1.2V supply voltage is performed. The results show an overall efficiency increase with a peak value of 62.8% comparing to 46.8% of a conventional one, and the output ripple voltage is reduced by nearly a half.

4.2.2 Tri-Charge Sharing Concept and The Proposed Clock Generator

The triple charge sharing (tri-charge sharing) concept is shown in Fig.4.15, where $C_1$ and $C_2$ are two capacitors of the same size representing the parasitics ($C_1=C_2=\alpha C$) driven by two out-of-phase clocks, while $C_s$ is a very large capacitor (comparing $C_1$ and $C_2$) used for charge storage. Initially, suppose $C_s$ has been charged to the steady state of $V_{dd}/3$, and $C_1$ is charged to $V_{dd}$ while $C_2$ is discharged to ground. In step 2, a connection opens between $C_s$ and $C_2$ that equalize their potential. Since $C_s$ is much larger than $C_2$, the voltage decrease on $C_s$ is negligible, and $C_2$ will also be charged to nearly $V_{dd}/3$ by $C_s$. In step 3, the connection between $C_s$ and $C_2$ is closed while a connection between $C_1$ and $C_2$ opens equalizing their potential on $2V_{dd}/3$. In step 4, the charge loss on $C_s$ in step 2 is compensated by $C_1$. Finally in step 5, $C_1$ is discharged to ground, while only a charge from $2V_{dd}/3$ to $V_{dd}$ on $C_2$ is required from the supply. In such a manner, the power consumption of the supply for each capacitor becomes $\alpha C f V_{dd}^2/3$. Comparing to the original value of $\alpha C f V_{dd}^2$ if no charge sharing scheme is utilized, the dynamic
4.2 Triple Charge Sharing Clock Scheme

Figure 4.15: Tri-charge sharing concept \((C_1=C_2=\alpha C)\).

Figure 4.16: Charge pump efficiency plot.
4. HIGH EFFICIENCY CHARGE PUMP CIRCUIT WITH 
CHARGE SHARING CLOCK SCHEME

Power consumption is reduced by two-thirds. In other words, the equivalent parasitic ratio is reduced to $\alpha/3$. Provided a charge pump circuit with such clock scheme, the efficiency boundary is able to achieve:

$$\eta_s = \frac{K}{N + 1 + \frac{\alpha}{3} \frac{N^2}{N+1-K}}, \quad (4.11)$$

and the theoretical efficiency comparison for $\alpha=0.2$ among original charge pump, dual-charge sharing charge pump and tri-charge sharing charge pump is shown in Fig.4.16.

Based on the tri-charge sharing concept, the proposed tri-charge sharing clock generator and the control signals are shown in Fig.4.17. The control signals are mainly obtained by the logic operation of input clock delay signals, $s1$, $s2$, $s3$ and $s4$:

$$en = s1 \odot s4,$$
$$c1 = (s1 + s4) \oplus (s2 + s3), \quad (4.12)$$
$$c2 = s2 \oplus s3,$$
$$c3 = (s1 \cdot s4) \oplus (s2 \cdot s3),$$

The driver enable signal $en$ is responsible for blocking the parasitics from the drivers during the charge sharing period. The switch control signals $c1$, $c2$ and $c3$ are used to achieve the charge sharing operation as shown in Fig.4.15. There should be proper non-overlapping period between each control signals so that the leakage current is able to be suppressed. The simulation result of the tri-charge sharing clock generator is shown in Fig.4.18. The potential disturb of the $C_s$ (dash line) during the charge sharing is relative to the size ratio between $C_s$ and $C_p$. The large the ratio, the smaller the disturb and more energy saving. However, for larger $C_s$ the potential setup time is longer and the area cost is another problem. For a ratio of 5 in our case, the average current consumption for the tri-charge sharing clock generator (including logic) is $18\mu A$. Comparing to the $48.5\mu A$ for the conventional clock without charge sharing, 62.9% power saving is achieved while the ideal case is 66.6%. If the ratio is enlarged to 10, the power saving is just 64.8%.
4.2 Triple Charge Sharing Clock Scheme

Figure 4.17: The proposed tri-charge sharing clock generator.

Figure 4.18: Simulation result of the proposed tri-charge sharing clock generator with comparison to the conventional clock without charge sharing ($V_{dd}=1.2$V, $f=1$MHz, $C_P=20$pF, $C_s=100$pF).
4. HIGH EFFICIENCY CHARGE PUMP CIRCUIT WITH CHARGE SHARING CLOCK SCHEME

4.2.3 Proposed Dual Charge Pump with Tri-Charge Sharing Clock Scheme

Since the outputs of a charge sharing clock generator are always out-of-phase while four phase overlapping clocks are generally utilized to minimize the charge pump switches loss, charge sharing clock scheme in one single charge pump circuit destroys the overlapping period, and deteriorate driving capability, especially for low voltage operation. In order to overcome the problem, a dual charge pump using two complementary sets of overlapping clocks is proposed, which is shown in Fig. 4.19.

The proposed 5-stage dual charge pump circuit is constructed by two branches with equal stage capacitance, and they work in a complementary manner so that the charge is delivered to the load by each branch in a different half clock period. The lower branch is mainly composed by NMOS stages, \(N_{stg}\). The charge transfer transistor \(N1\) and the auxiliary transistor \(N2\) together with a small charge blocking capacitor \(C_g\), usually around 1% of \(C\), fulfill the threshold cancellation in the same manner as the conventional NMOS four phase charge pump circuit [3]. Transistor \(Nb\) is used to track the body of \(N1\) to a lower potential so that the body-effect is eliminated. The upper branch of the proposed double charge pump is mainly composed by PMOS stages, \(P_{stg}\). The \(P_{stg}\) is complementary to the \(N_{stg}\), and the operation of upper branch is also complementary to the lower one. The \(P_{stg}\) in lower branch is used to eliminate the output loss because \(N_{stg}\) would malfunction if the potential of node \(nh\) is fixed. Similarly, a \(N_{stg}\) is used as the input stage of the upper branch.

The \(N\)-set clock with overlapping-high period between \(clk1\) and \(clk2\) is used to feed the lower NMOS branch, while the \(P\)-set clock with overlapping-low period between \(clk1'\) and \(clk2'\) is used to feed the upper PMOS branch. The \(clk1\) and \(clk1'\), \(clk2\) and \(clk2'\) are two pair of complementary clocks produced by two tri-charge sharing clock generator shown in Fig. 4.17. The \(clk3\) and \(clk3'\), \(clk4\) and \(clk4'\) are also complementary, however, since capacitor \(C_g\) is very small comparing to \(C\), usually around 1%, the parasitics of \(C_g\) is negligible and charge sharing is unnecessary.
4.2 Triple Charge Sharing Clock Scheme

Figure 4.19: Proposed 5 stage double charge pump.
4. HIGH EFFICIENCY CHARGE PUMP CIRCUIT WITH CHARGE SHARING CLOCK SCHEME

4.2.4 Simulation Results

To evaluate the proposed tri-charge sharing scheme, simulation under 0.18µm technology is performed and the parameters are summarized in the following:

The charge storage capacitor $C_s$ is set to be 5 times of the parasitics loading each clock. Since the parasitic on $clk1$ and $clk1'$ are both 30pF (50pF × 3 × 0.2), the $C_s$ of the tri-charge sharing clock generator for those two clocks is 150pF, and for $clk2$ and $clk2'$, the $C_s$ is 100pF. For comparing reason, simulations with the same parameters are also performed on a conventional single branch four-phase charge pump without charge sharing.

Fig.4.20 shows the output voltage and the current consumption for 200KΩ load condition. For the output voltage, both of the proposed and conventional charge pump are able to reach the same level about 5.7V, however, owing to the double branch architecture, the ripple voltage of the proposed charge pump is only 54mV comparing to 121mV for the conventional one. As for the supply current, the peak value for conventional charge pump is over 9mA while it is less than 3mA for the proposed tri-charge sharing charge pump.

The output characteristic and ripple voltage comparison for different load conditions are shown in Fig.4.21. The V-I curve of the proposed charge pump follow closely to that of the conventional one, while the output voltage becomes a little higher in heavy load conditions. This result suggests that the four-phase threshold cancellation scheme works normally for the proposed tri-charge sharing clock scheme, and the driving capability has not declined. The ripple voltage is

<table>
<thead>
<tr>
<th>Table 4.2: Main Design Parameters.</th>
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<tr>
<td>Technology</td>
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<tr>
<td>Stage number $N$</td>
</tr>
<tr>
<td>Supply voltage $V_{dd}$</td>
</tr>
<tr>
<td>Clock frequency $f$</td>
</tr>
<tr>
<td>Boost capacitance $C_g$</td>
</tr>
<tr>
<td>Pumping capacitance $C$</td>
</tr>
<tr>
<td>Load capacitance $C_L$</td>
</tr>
<tr>
<td>Parasitic ratio $\alpha$</td>
</tr>
</tbody>
</table>
4.2 Triple Charge Sharing Clock Scheme

![Graph 1: Output voltage and supply current comparison for 200KΩ load condition.](image1)

**Figure 4.20:** Output voltage and supply current comparison for 200KΩ load condition.
4. HIGH EFFICIENCY CHARGE PUMP CIRCUIT WITH CHARGE SHARING CLOCK SCHEME

Figure 4.21: V-I characteristic and ripple voltage comparison.

an important concern for many applications, especially for non-volatile memory. Owing to the double branch architecture, nearly 50% ripple reduction is achieved. Although smaller ripple can be obtained by enlarging the decoupling capacitance $C_L$, it leads to long set-up time and large area penalty.

The power efficiency is calculated by the following equation:

$$\eta = \frac{P_{out}}{P_{in} + P_{drv} + P_{csh}}.$$  \hspace{1cm} (4.13)

where $P_{out}$ is the output power, $P_{in}$ is the input power, $P_{drv}$ is the clock driving power and $P_{csh}$ is the extra power of the proposed tri-charge sharing clock generator which is not included in the calculation of the conventional charge pump. The power efficiency comparison is shown in Fig.4.22. The proposed tri-charge sharing charge pump shows a overall efficiency increase, and the peak value is 62.8% comparing to 46.8% of the conventional one.

4.3 Conclusion

In this chapter, the power efficiency of charge pump circuits is discussed, and a dual charge pump circuit with complementary architecture using charge sharing clock scheme is designed. The proposed double charge sharing clock generator is able to recover half of the charge from parasitic-capacitor charging and discharging, so that the dynamic power loss in the pumping process is reduced by
a half. Test chip is also fabricated in 0.18\(\mu m\) CMOS process with a bottom plate parasitic ratio around 0.1, The area penalty of the charge sharing generator is less than 1%. Measurements under 1V, 1.2V and 1.5V supply conditions are conducted. The results show an overall efficiency increase with 11% in the peak value, and no driving capability decline occurs in all cases, while the ripple voltage is reduced by a factor of about 43% comparing the conventional single branch charge pump circuit. For the triple charge sharing, the dynamic power consumption during the pumping period is reduced by nearly two-thirds. Simulation results for a parasitic ratio of 0.2 show an overall efficiency increase with a peak value of 62.8% for the proposed charge pump comparing to 46.8% for the conventional one, and the output ripple voltage is also reduced by nearly a half without enlarging the decoupling capacitance.

\[ \text{Figure 4.22: Power efficiency comparison.} \]
4. HIGH EFFICIENCY CHARGE PUMP CIRCUIT WITH CHARGE SHARING CLOCK SCHEME
In this chapter, an area efficiency hybrid decoupling scheme is proposed to suppress the charge pump noise during F-N tunneling program in non-volatile memory (NVM). The proposed scheme is focused on suppressing the average noise power in frequency domain aspect, which is more suitable for the program error reduction in NVMs. The concept of active capacitor is utilized. Feed forward effect of the amplifier is firstly considered in the impedance analysis, and a trade-off relation between in-band and out-band frequency noise decoupling performance is shown. A fast optimization based on average noise power is made to achieve minimum error in the F-N tunneling program. Simulation results show very stable output voltage in different load conditions, the average ripple voltage is 17mV with up to 20dB noise-suppression-ratio (NSR), and the F-N tunneling program error is less than 5mV for a 800\(\mu\)s program pulse. A test chip is also fabricated in 0.18\(\mu\)m technology. The area overhead of the proposed scheme is 2%. The measurement results show 24.4mV average ripple voltage compared to 72.3mV of the conventional one with the same decoupling capacitance size, while the noise power suppression achieves 15.4dB.
5. LOW NOISE CHARGE PUMP CIRCUIT WITH HYBRID DECOUPLING SCHEME

5.1 Introduction

Non-volatile memories (NVMs) have been widely adopted in various applications such as PDAs and SSDs these years [21, 32]. Generally, a charge pump (CP) circuit is implemented to provide the programming or erasing high voltage. One of the main design concerns in CP circuits is the ripple noise, which increases the chance of over programmed cells decreasing the bit error rate [29, 33]. Conventional NVMs with high programming voltage over 15V have a relatively wide $V_{th}$ distribution window, and the $V_{th}$ control is mainly covered by various verifying schemes [34, 35]. However, new devices using high-$k$ materials and others such as SONOS or ferroelectric NVMs have scaled the programming voltage to around 7V, resulting in a much narrower $V_{th}$ distribution window [20, 36, 37], and multi-level-cell (MLC) technology have also made the $V_{th}$ range for each state as well as the reliable margin decrease to the order of several hundreds mV [38]. Such that an more accurate program is desirable in order not to compromise too much of the data throughput due to excessive verifying process [39]. As a result, the noise suppression in CP circuits becomes more important and indispensable.

Since the CP ripple noise is mainly caused by the current mismatch between output and the load, most noise suppression techniques are based on improving the feed-back regulation loop [27]. A by-pass capacitor is added to the resistive divider to decrease the $RC$ delay of noise sampling in [40], while the regulation level becomes unstable for different load condition. A skipping-based regulation dynamically changing the size of output transistor is described in [41] to smooth the current output, while it is two phase CP oriented. And a pumping current and frequency control scheme adjusting the output current according to the load is proposed in [30], while the area overhead is quite large. Despite of their effectiveness and drawbacks, since the regulation speed is always limited, a large decoupling capacitor at the output is still required for noise filtering in all cases. Besides, if further noise suppression is desired, enlarging the decoupling capacitance becomes the only method, and large area overhead and long set-up time become the problems. In addition, conventional CP noise suppression is only focused on ripple voltage reduction, whereas the average noise power is more relative to the program accuracy in NVMs.
To solve these problems, a hybrid decoupling scheme using both active and passive capacitors is proposed for CP noise suppression in NVMs. The active capacitor technique is originally used for noise reduction in digital ICs [42, 43], where the equivalent decoupling capacitance is boosted several times by Miller-effect with smaller capacitor size. Because of the difference between the noise in CPs and digital ICs, analysis of the decoupling impedance for CP noise is performed. The amplifier feed-forward effect is firstly considered in this paper, and a trade-off relation between in-band and out-band frequency decoupling performance is shown, then, an optimization on average noise power is made to achieve minimum F-N tunneling program error. Simulations show that the proposed optimized scheme with 20pF total decoupling capacitance is able to achieve nearly the same ripple of 17mV as conventional 100pF decoupling without set-up time sacrifice, while the average noise power is even smaller. The simulated F-N program error is less than 5mV for the proposed scheme while it is 0.03V and 0.2V for conventional 100pF and 20pF decoupling. Test chip of a hybrid decoupling charge pump and a conventional one with same capacitance are fabricated in 0.18\(\mu\)m technology. The measurement results show 24.4mV average ripple voltage compared to 72.3mV with an NSR of 15.4dB. Since the proposed decoupling scheme is independent on the regulation, it can be combined with any other techniques based on the feedback.

### 5.2 Analysis and Optimization of Hybrid Decoupling Scheme

#### 5.2.1 Impedance Analysis

The concept of hybrid decoupling scheme is shown in Fig.5.1-a). The passive decoupling path is formed by a capacitor \(C_p\), and the active decoupling path is composed by a capacitor \(C_a\) and an amplifier, of which the transfer function is simplified as:

\[
A(s) = \frac{-G_m R_o}{1 + s/\omega_o} = \frac{-A}{1 + s/\omega_o},
\]

(5.1)
5. LOW NOISE CHARGE PUMP CIRCUIT WITH HYBRID DECOUPLING SCHEME

where \( G_m \) is the transconductance, \( R_o \) is the equivalent output resistance and \( \omega_o \) is the first pole.

For digital ICs, since the substrate crosstalk and supply noise are mainly caused by coupling effect or stray inductance, the noise spectrum is highly concentrated around certain frequency in the order of hundreds MHz, and large capacitor in several pF order is used to improve the amplifier bandwidth to contain most of the noise spectrum, such that only in-band Miller effect is considered and \((1 + A(s))C_a\) is taken to be the effective capacitance in their analysis [42, 43].

However, noise in charge pump circuits is caused by the current mismatch between the output and load, which results in a relatively flat low-pass type spectrum, and an example is shown in Fig. 5.2. On the other hand, since the noise on CP output should be sampled to the amplifier input range, a divider is used, so that the amplifier gain should be enhanced to compensate for the attenuation while sacrificing the bandwidth. As a result, noise decoupling outside the bandwidth must be analyzed.

As the gain degrades with the increase of frequency, the feed-forward effect becomes significant. For the circuit in Fig. 5.1-a), this means more signals are to directly pass through \( C_a \) rather than being amplified. Taking this effect into consideration, the noise current which flows through \( C_a \) is:

\[
I_a(s) = sC_aV_a(s) \left[ 1 + \frac{G_mR_o}{(1 + \frac{s}{\omega_o})(1 + \frac{s}{\omega_1})} - \frac{R_o}{R_o + \frac{1}{sC_a}} \right],
\]

\[
\frac{I_a(s)}{V_a(s)} = \frac{1}{\frac{s}{\omega_o\omega_1AC_a} + \frac{\omega_o\omega_1}{AC_a} + \frac{1}{sC_a}} + \frac{1}{R_o + \frac{1}{sC_a}},
\]

Figure 5.1: The hybrid decoupling scheme and equivalent circuit.
5.2 Analysis and Optimization of Hybrid Decoupling Scheme

Figure 5.2: Noise spectrum of a conventional decoupling charge pump.

where $\omega_1 = (R_oC_a)^{-1}$. Since $C_a$ is very large compare to the capacitance in the amplifier, $\omega_1$ is usually smaller than $\omega_o$. It can also be proved that even if the amplifier has an infinity bandwidth ($\omega_o \rightarrow \infty$), the Miller-effect is still band limited by $\omega_1$.

By rearranging Eq.(5.2) and take $C_p$ into calculation, the impedance for hybrid decoupling scheme is obtained:

$$Z_h(s) = \frac{V_a(s)}{I_a(s)} \| \frac{1}{sC_p}$$

$$= (sL_e + R_e + \frac{1}{sAC_a})\|(R_o + \frac{1}{sC_a})\| \frac{1}{sC_p}$$

(5.4)

where the effective inductance and resistance are found to be:

$$L_e = \frac{1}{\omega_o\omega_1AC_a} = \frac{1}{\omega_oG_m}$$

(5.5)

$$R_e = \frac{\omega_o + \omega_1}{\omega_o\omega_1AC_a} = \frac{1}{\omega_oAC_a} + \frac{1}{G_m} \ll R_o.$$  

(5.6)

The equivalent circuit is shown in Fig.5.1-b). The hybrid ratio $\beta \in [0, 1]$ is defined to describe the relation between active and passive decoupling paths, which is:

$$C_a = \beta C_L$$

$$C_p = (1 - \beta)C_L.$$  

(5.7)
Notice two special situations here, that \( \beta = 0 \) corresponds to the conventional fully passive decoupling, and \( \beta = 1 \) corresponds to the fully active decoupling.

The impedance characteristic of the hybrid decoupling scheme is shown in Fig. 5.3. For \( \omega < \omega_1 \), as \( \beta \) rises, the decoupling impedance decreases indicating a better decoupling performance. Since Miller effect is dominant in this region, the equivalent capacitance is nearly \( (1 + A)C_a \) and the noise is mainly decoupled by the active path. Within \( \omega_1 \) and \( (A\omega_1\omega_1)^{1/2} \), the effect of \( L_e \) becomes obvious, a local minimum impedance occurs near the resonant frequency of \( L_e \) and \( C_a \) (in parallel), and a local maximum occurs near the resonant frequency of \( L_e \) and \( AC_a \) (in series). Beyond \( (A\omega_1\omega_1)^{1/2} \), the noise is mainly decoupled by \( C_p \), and the decoupling impedance increases with the rise of \( \beta \). As for \( \beta = 1 \), the fully active decoupling case, since feed-forward effect is significant for higher frequency, and there is no other optional path to decouple the noise current, the impedance finally turns into a resistor \( R_o \), which is also the reason why a passive decoupling path is added for charge pump circuit.
5.2 Analysis and Optimization of Hybrid Decoupling Scheme

5.2.2 Impedance Optimization

For a charge pump circuit, a well-performed hybrid decoupling scheme relies on many aspects while some are of key importance such as the gain $A$ and the bandwidth $\omega_o$ of the amplifier, the total decoupling capacitance $C_L$, and the decoupling ratio $\beta$. The goal of the optimization is to properly configure these parameters achieving the lowest noise level.

The influence of gain $A$ and $\omega_o$ to the decoupling impedance is depicted in Fig.5.4. An increase in $A$ results in a better low frequency noise performance, while a large $\omega_o$ just smooth the impedance increase from $(\omega_o \omega_1)^{1/2}$ to $(A\omega_o \omega_1)^{1/2}$. However, the decoupling performance improvement from increasing $\omega_o$ is limited comparing to that from increasing $A$, and considering the trade-off between gain and bandwidth, as well as the fact that a divider (with a gain less than 1) is to be used before the amplifier to sample the noise, a large amplifier gain is preferred, while an $\omega_o$ of several times larger than $\omega_1$ is adequate.

For the total capacitance $C_L$ and the decoupling ratio $\beta$, although the size of $C_L$ is somehow limited by the area constrain, the noise suppression performance varies a lot with different choice of $\beta$. The hybrid ratio $\beta$ is a parameter by which the balance between passive and active decoupling strength is adjusted. Provided a certain $C_L$, a larger $\beta$ indicates a better in-band frequency ($< \omega_1$) performance at the cost of sacrificing the out-band frequency ($> \omega_1$) performance.

Figure 5.4: Influence of $A$ and $\omega_o$ to the decoupling impedance.
vice versa. And by an appropriate choice of \( \beta \), the lowest noise level can be achieved. Conventionally, the charge pump noise is measured in ripple voltage, however, the impedance analysis is in frequency domain making the expression for ripple voltage in time domain quite implicit. More important, the ripple voltage during program does not affect the \( V_{th} \) distribution directly in NVMs, it disturbs the F-N tunneling current, and the threshold voltage shift is proportional to the quantity of injection charge, which is the integration of the F-N current over time \([44]\). Thus, the average noise power is a more effective measurement to determine the CP noise impact on NVMs. The average noise power of hybrid decoupling CP can be expressed as a function of \( \beta \):

\[
P_n(\beta) = \int_0^\infty |\Delta I^2(j\omega) \cdot Z_h^2(j\omega, \beta)| \, d\omega, \tag{5.8}
\]

where \( \Delta I^2(\omega) \) is the noise current PSD (Power spectrum density), and \( P_n \) is expressed in \( V^2 \). The optimum \( \beta \) can then be obtained according to following equation:

\[
\frac{dP_n(\beta)}{d\beta} = 0. \tag{5.9}
\]

However, Eq.(5.8) and (5.9) are mathematical, not practical for calculation, since \( \Delta I(j\omega) \) is not analytic and is uncertain until the decoupling scheme is constructed. Besides, a full sweep simulation on \( \beta \) for a hybrid decoupling CP takes hours or more according to the complexity. Alternatively, taking advantage of the property that the change of \( \Delta I(j\omega) \) must be continuous, as the fact for most physical quantities, the optimum \( \beta \) can be calculated in the following process numerically:

1 \ : \ set \ \beta_1 = 0;
2 \ : \ run \ \text{Spice} \ \text{simulation} \ \text{to} \ \text{get} \ |\Delta I_{\beta_1}(j\omega_s)|;
3 \ : \ \text{for} \ \beta = 0 \ \text{to} \ 1, \ \delta_\beta++

\[
P(\beta) = \sum_1^N |\Delta I_{\beta_1}(j\omega_s)Z_h(j\omega_s, \beta)|^2;
\]

\end

\text{end};\]

\text{find} \ P(\beta_2) = min[P(\beta)];
4 \ : \ \text{if} \ |\beta_2 - \beta_1| > \delta_\beta \tag{5.10}
5.3 Circuit Implementation of the Proposed Hybrid Decoupling Charge Pump

\[
\beta_1 = \beta_2, \text{ and go back to step 2;}
\text{else}
\beta_o = \beta_2 \text{ (optimum } \beta); \text{end;}
\]

where \(\omega_s\) is the sampling frequency, \(N\) is the sample length, and \(\delta_\beta\) is the step for noise power calculation. The sampling frequency \(\omega_s\) and length \(N\) must be large enough to minimize the calculation error. The smaller the \(\delta_\beta\), more accurate optimum \(\beta\) is. Since the noise power is usually measured in dB scale, a \(\delta_\beta\) of 0.05 is enough, and the result converges in about 2 or 3 iterations, which means only 2 or 3 rounds of simulation are required comparing to 20 rounds at 0.05 step for a full \(\beta\) sweep. The optimization result is shown in the next section.

5.3 Circuit Implementation of the Proposed Hybrid Decoupling Charge Pump

To prove the effectiveness of the proposed hybrid decoupling scheme for CP noise suppression, a hybrid decoupling charge pump circuit is designed, shown in Fig.5.5. The capacitor \(C_p\) forms the passive decoupling path, while the active decoupling path is composed by a resistive divider, an active amplifier and a capacitor \(C_a\). The supply voltage for the design is 1V.

Fig.5.6 shows the charge pump circuit. The four phase threshold voltage cancellation scheme is utilized to improve the efficiency [3]. In order to solve

![Figure 5.5: Proposed hybrid decoupling charge pump.](image-url)
5. LOW NOISE CHARGE PUMP CIRCUIT WITH HYBRID DECOUPLING SCHEME

Figure 5.6: Proposed 8-stage charge pump circuit.

the body effect problem, a PMOS charge transfer block is proposed, the p-stage shown in Fig.5.6. The charge transfer transistor M1 and the auxiliary transistor M2 together with $C_g$ realize the threshold cancellation, and the size of $C_g$ is about 1% of the pumping capacitor $C$. Transistor Mb is used to control the body potential. The gate of Mb is bounded to the gate of M1. When M1 is turned on to transfer charge from node $S$ to $D$, Mb is also turned on so that the body of M1 is short to its source, and the body effect of M1 is eliminated during this period. When M1 is turned off in the charge block phase, Mb is also turned off, so that M1’s body can be coupled to a potential high enough to prevent charge flowing back from M1’s drain to source. The input stage remains NMOS type in that the threshold cancellation scheme fails if the source side of the p-stage is connected to a fixed potential.

According to the charge pump optimization theory $[25]$, to achieve maximum efficiency, the optimum stage number should be:

$$N_o = \left(1 + \sqrt{\frac{\alpha}{1+\alpha}}\right) \left(\frac{V_{out}}{V_{dd}} - 1\right) \quad (5.11)$$

where $\alpha$ is the parasitic ratio. In our design, the output voltage of the charge pump is regulated at 7V, voltage supply is 1V, and $\alpha$ is nearly 0.1. Therefore, the optimum stage number is found to be 8.
5.3 Circuit Implementation of the Proposed Hybrid Decoupling Charge Pump

Figure 5.7: The active amplifier \((C2=C3=100fF, C1=150fF)\).

Figure 5.8: Simulated bode plot of the amplifier.

Figure 5.9: The comparator.
5. LOW NOISE CHARGE PUMP CIRCUIT WITH HYBRID DECOUPLING SCHEME

The active amplifier is shown in Fig.5.7, in which $C_1$, $C_2$ and $C_3$ are small capacitors in the order of fF used for nested Miller compensation. The first stage is in unity gain configuration to ameliorate the bandwidth. Since the supply voltage is only 1V, a class AB buffer with the adaptive load scheme is implemented as the output stage to acquire enough output dynamic range as well as small current consumption\[45\]. The simulation result of the amplifier is shown in Fig.5.8. The comparator is shown in Fig.5.9. To avoid the need of too many reference voltages, all the biases in the amplifier and comparator are designed in the same level. Comparing the proposed circuit shown in Fig.5.5 with the conventional one, the area penalty only lies in the amplifier, which occupies just a very small percentage in the whole system since no large capacitor is adopted.

5.4 Results and Discussion

The main design parameters are summarized in the following table 1:

<table>
<thead>
<tr>
<th>Table 5.1: Main Design Parameters</th>
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<tbody>
<tr>
<td>Technology</td>
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<tr>
<td>Supply voltage $V_{dd}$</td>
</tr>
<tr>
<td>Regulation level $V_{out}$</td>
</tr>
<tr>
<td>Clock frequency $f$</td>
</tr>
<tr>
<td>Pumping capacitance $C$</td>
</tr>
<tr>
<td>Total decoupling capacitance $C_L$</td>
</tr>
<tr>
<td>Optimum hybrid ratio $\beta_o$</td>
</tr>
<tr>
<td>Active capacitance $C_a$</td>
</tr>
<tr>
<td>Passive capacitance $C_p$</td>
</tr>
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</table>

The optimum hybrid ratio $\beta_o$ is calculated by algorithm (5.10). The sampling frequency $\omega_s$ is 500MHz, total length $N$ is 20000 points and the calculation step $\delta_\beta$ is 0.05. The iteration process is shown in Fig.5.10. The initial iteration start with the noise current PSD at $\beta=0$ obtained by simulation, and the minimum noise power is found to be at $\beta=0.25$. Next, the second iteration start with $\beta=0.25$, and since the minimum noise power is found to be at the same point,
0.25 is chosen as the optimum hybrid ratio $\beta_o$. In this case, the result converges in only 2 iterations, comparing to a full $\beta$ sweep simulation of 20 (1/0.05) rounds which may take hours, the speed is very fast.

To verify the calculated optimum $\beta_o$, simulation for different $\beta$ value is performed, and the results are shown in Fig.5.11. The legend is constant for the two figures. The solid black line of $\beta=0$ represents the conventional passive decoupling which has a ripple about 65mV. The dash line of $\beta=1$ represents the fully active decoupling, and the high frequency noise is very large over 0.2V. The red line with optimum $\beta_o=0.25$ only has a ripple of about 18mV, and the noise power calculated from the PSD figure is the lowest. For larger $\beta$, the noise in lower frequency domain is smaller while more higher frequency noise occurs, and the variation of noise distribution with $\beta$ is in accordance with Fig.5.3, which proves the validity of our optimization.

The charge pump set-up time is a very important factor in the NVM applications, and a faster set-up improves the program speed. The simulation result for set-up time is shown in Fig.5.12. To simplify the expression, $\beta@C_L$ format is used to describe the decoupling configurations. $\beta=0@100pF$ indicates a conventional passive decoupling with 100pF decoupling capacitance, and $\beta=0.25@20pF$ indicates a hybrid decoupling scheme with $\beta=0.25$ and 20pF total decoupling capacitance. For conventional passive decoupling, the ripple voltage and set-up
5. LOW NOISE CHARGE PUMP CIRCUIT WITH HYBRID DECOUPLING SCHEME

Figure 5.11: Output noise transient and PSD at 1μA load.

time are always trade-off. Although the β=0@100pF case has small ripple voltage, the set-up time is long about 110μs. The β=0@20pF case has short set-up time about 40μs but the ripple voltage is quite large. The hybrid decoupling case of β=0.25@20pF, however, has both small ripple voltage, nearly the same as the β=0@100pF case, and short set-up time, nearly the same as the β=0@20pF case.

For NVM applications, a stable program voltage for different load condition is necessary, since the number of cells in each program operation is not necessarily the same. If the program voltage varies a lot with the load, the program accuracy is low, and more error bits occur. Shown in Fig.5.13-a) is the average output voltage for three different decoupling configurations. In all cases, the 7V
5.4 Results and Discussion

Figure 5.12: Charge pump set-up time test.

Figure 5.13: Output characteristic and noise performance
regulation level is broken when the load current is larger than 3.3µA (the program current of F-N tunneling for each cell is in the order of several nA). The maximum DC deviation is defined as the maximum difference between average output voltage and the regulation level, which is about 1mV for $\beta=0.25@20pF$ case, nearly 2mV for $\beta=0@100pF$ case and 20mV for $\beta=0@20pF$ case. Small ripple voltage is also very important for NVMs because the F-N tunneling current is nearly exponentially dependent on the program voltage. The ripple voltage comparison is shown in Fig.5.13-b). The average value for $\beta=0.25@20pF$ and $\beta=0@100pF$ case are nearly the same about 17mV, while it is around 70mV for $\beta=0@20pF$ case. Comparing those three decoupling configurations, the proposed hybrid decoupling charge pump is able to produce stable output with small ripple at a very low area cost.

As is analyzed in Eq.(5.8) and (5.9), the average noise power is the most effective measurement to tell the accuracy of the program operation, and the results are shown in Fig.5.13-c), where NSR (Noise-Suppression-Ratio) is the average noise power ratio in dB scale between two samples. For comparison reason, the $\beta=0@20pF$ case is chosen to be a basis. The NSR of $\beta=0.25@20pF$ is around 18dB and maximum 20dB, while it is around 13dB for $\beta=0@100pF$ case. This result indicates that even the stability and ripple voltage is the same for $\beta=0.25@20pF$ and $\beta=0@100pF$, the program accuracy of the hybrid decoupling case is higher.

To better evaluate the proposed hybrid decoupling charge pump, simulation on $V_{th}$ shift by F-N tunneling is performed. For floating gate NVM with $SiO_2$ as insulator, the F-N current density has the form [44]:

$$J_{FN}[A/m^2] = 1.15 \times 10^{-6} E_{inj}^2 \cdot \exp \left[ -\frac{2.54 \times 10^{10}}{E_{inj}} \right]$$

$$E_{inj} = \frac{\alpha_g V_g}{t_{ox}}, \quad (5.12)$$

where $\alpha_g$ is the GCR(Gate-Coupling-Ratio), $V_g$ is the program voltage on control gate and $t_{ox}$ is the tunneling oxide thickness. And the $V_{th}$ shift is expressed as:

$$\Delta V_{th} = \int_0^t J_{FN} \cdot \frac{dt}{\epsilon_I} \cdot d_I, \quad (5.13)$$
where \( d_I \) is the distance from charge storage location to the gate, and \( \epsilon_I \) is the dielectric constant of the insulator. The worst case programming curve is shown in Fig.5.14. The dotted line is the result for an ideal 7V program. For a 800\( \mu \)s pulse, the program error for passive decoupling \( \beta = 0@20pF \) is the largest, about 0.23V, in other words, the \( V_{th} \) distribution under such decoupling will be widened by 0.23V, which is un-acceptable for low voltage NVMs, especially those MLCs. By enlarging the decoupling capacitance, the \( \beta = 0@100pF \) case has reduced the program error to 0.03V. However, the program error of the proposed hybrid decoupling \( \beta = 0.25@20pF \) is less than 5mV with only one fifth decoupling capacitance of \( \beta = 0@100pF \) case.

To further prove the validity, a hybrid decoupling charge pump of \( \beta = 0.25@20pF \) and a conventional decoupling charge pump of \( \beta = 0@20pF \) are also fabricated in 0.18\( \mu \)m process. The die photograph of \( \beta = 0.25@20pF \) case is shown in Fig.5.15. The total area is 0.175mm\(^2\). The only area overhead lies in the amplifier which only occupies about 2% area. Fig.5.16 shows the output voltage of the charge pump circuit, the red line is for the output voltage and the green line is for the input clock. As the clock starts, the charge pump is able to achieve the pre-defined
5. LOW NOISE CHARGE PUMP CIRCUIT WITH HYBRID DECOUPLING SCHEME

7V regulation level. The measured output noise and its spectrum are shown in Fig.5.17. The red line is the waveform for the proposed hybrid decoupling charge pump and the green line is for the conventional one. The ripple voltage for conventional decoupling is 72.3mV, while the average ripple voltage for the proposed hybrid decoupling is about 24.4mV. The difference between simulation and measurement results may cause by the supply and reference variation which affects the performance of active amplifier and comparator, and is not considered in simulation. The noise suppression in frequency domain is more obvious. The spectrum for the proposed scheme is suppressed under 2mV from 12mV of the conventional case, and an NSR of 15.4dB is calculated from the spectrum root-mean-square(rms). The maximum output current within 7V regulation level is about 3µA. If larger current is required, larger pumping capacitance or faster

**Table 5.2:** Ripple reduction comparison.

<table>
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<td>65nm</td>
<td>0.7µm</td>
<td>0.13µm</td>
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<tr>
<td>$V_{dd}$</td>
<td>1V</td>
<td>1.5V</td>
<td>3V</td>
<td>3.3V</td>
</tr>
<tr>
<td>$V_{out}$</td>
<td>7V</td>
<td>14.5V</td>
<td>5V</td>
<td>4.5-5V</td>
</tr>
<tr>
<td>$f$</td>
<td>2MHz</td>
<td>20MHz</td>
<td>0.1MHz</td>
<td>0.4-0.6MHz</td>
</tr>
<tr>
<td>$C_l$</td>
<td>20pF</td>
<td>N/A</td>
<td>1µF</td>
<td>2µF</td>
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<tr>
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<td>96mV</td>
<td>N/A</td>
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<td>0.2V</td>
<td>44.6mV</td>
<td>33.8mV</td>
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</table>
5.4 Results and Discussion

Figure 5.16: Charge pump output voltage setup.

Figure 5.17: Measured output noise at 1µA load.

clock is needed. And sometimes, several sets of identical charge pump circuits are parallely connected to improve the driving capability. In each case, however, the optimum $\beta_o$ must be re-calculated since the parameters have changed. The ripple reduction comparison with different noise suppression techniques is shown in the following table.

Although our discussion here is only based on 7V noise decoupling, the proposed decoupling scheme is not limited by the charge pump output voltage, since the analysis in previous section is independent on the charge pump topology. For the architecture shown in Fig.5.5, higher output voltage can be obtained by
5. LOW NOISE CHARGE PUMP CIRCUIT WITH HYBRID DECOUPLING SCHEME

Figure 5.18: Simulation result of a 15V-output charge pump at 1μA load current (C.P. stages=16, C=10pF, CL=20pF, β_o=0.3)

adding more p-stages in the charge pump circuit and properly adjusting the divider ratio. As an example, simulation is performed on a 16-stage charge pump with 15V regulation level, which is required for most commercial NAND flash memory, and the result is shown in Fig.5.18 for reference. However, it should be notice that if the divider ratio is very small, the gain attenuation becomes large, and the gain of amplifier should be further enhanced to compensate the effect, which is a difficulty for noise decoupling on high output voltage in low supply.

5.5 Conclusion

A hybrid decoupling scheme is proposed to suppress the program noise of charge pump circuits in non-volatile memory applications. The amplifier feed-forward effect is firstly considered in the decoupling impedance analysis, and a fast optimization is made to achieve maximum noise suppression performance. The proposed hybrid decoupling scheme focuses on the average noise power suppression, which is more effective for program accuracy improvement in NVMs, and the simulated $V_{th}$ shift error for a 800μs program pulse by F-N tunneling is less than 5mV. The test chip is fabricated in 0.18μm technology, and the area over head of the proposed scheme is only 2%. The measurement results show an average
ripple voltage of 24.4mV comparing to 72.3mV of the conventional decoupling with 15.4dB NSR. The decoupling performance of the proposed scheme can be boosted by increasing the amplifier’s gain instead of enlarging the decoupling capacitance. Besides, since the proposed decoupling scheme is independent on the regulation, it is able to be combined with any other techniques based on the feed back.
5. LOW NOISE CHARGE PUMP CIRCUIT WITH HYBRID DECOUPLING SCHEME
6 Conclusions and Future Works

6.1 Conclusions

In this thesis, the charge pump circuits for non-volatile memory are discussed. The theoretical analysis of the mathematical model and the design obstacles are presented. We have shown the methods to solve the threshold voltage and body effect problem in designing a good charge transfer unit. The efficiency and noise problems in low operation voltage are intensively addressed.

To improve the charge pump efficiency, a complementary charge pump architecture with charge sharing clock scheme is proposed to recover part of the dynamic loss during the pumping process, and the charge sharing order can be double, triple or even quadruple. A charge pump circuit with double charge sharing clock scheme is fabricated in 0.18\(\mu\)m technology with a parasitic ratio of 0.1, and the measurement results shows more than 10% peak efficiency increase with no drivability decline. Simulations on a triple charge sharing charge pump circuit with 0.2 parasitic ratio are also performed to prove the validity, and the results show over 15% peak efficiency improvement. The charge sharing concept is also extended to triple charge sharing scheme. A dual charge pump circuit with triple charge sharing clock scheme is described. The proposed triple charge sharing clock generator is able to recover nearly two-thirds of the charge from the parasitics charging, in which way the dynamic power loss in the pumping process is reduced to almost one-third. Under 0.18\(\mu\)m technology with a bottom plate parasitic ratio of 0.2, the simulation results of a proposed 5-stage charge pump
6. CONCLUSIONS AND FUTURE WORKS

circuit show an overall efficiency increase with a peak value of 62.8% comparing to 46.8% of a conventional one, and the output ripple voltage is reduced by nearly a half.

To suppress the charge pump noise, a hybrid decoupling scheme using both active decoupling and passive decoupling methods is proposed to suppress the noise power without output capacitance increase. The concept of active capacitor is utilized. Feed forward effect of the amplifier is firstly considered in the impedance analysis, and a trade-off relation between in-band and out-band frequency noise decoupling performance is shown. A fast optimization based on average noise power is made to achieve minimum error in the F-N tunneling program. Test chip is also fabricated in 0.18µm technology. The measurement results shows more than 15.4dB noise suppression improvement with the same output capacitance. The hybrid decoupling scheme is extremely useful when the output voltage set-up time and the area cost are critical factors to the system.

6.2 Future Works

For practical utilization of the charge sharing scheme, the regulation effect must be taken into consideration. The efficiency boundary equation shown in Chapter 4 is obtained under the un-regulated condition, which guarantee a linear relation between the output voltage and the output current (Eq.2.7). However, if regulation is introduced, this relation is no longer valid since the output voltage is fixed to the regulation level. The regulation would also influence the charge sharing operation. For the common on/off regulation strategy, the clock drivers are all turned off if the output voltage exceeds the regulation level, which results in two effects. The first one is that the clock inputs would change between \( V_{dd} \) and \( GND \) several time in one period indeterminately, and those indeterminate changes can hardly be scheduled for charge sharing. The second effect is that the regulation would interrupt the charge sharing operation if the turn-off occurs during the sharing process. One possible solution is the clock frequency modulation. Since the clock frequency varies according to the output current, an linear relation between the clock dynamic loss and the output current is established, which in turn provides the possibility to locks the efficiency to the top point. Also, since the
6.2 Future Works

no extra on/off occurs in one clock period, the charge sharing scheme is able to be implemented without much changes.

One remaining topic of the proposed hybrid decoupling scheme lies in the output sampling method. In the proposed scheme, a simple resistive divider is used at the cost of gain attenuation and GBW decrease in the feedback. Provided a 10V output with a 1V reference, the attenuation is 20dB with the GBW decreased by one dec, which means even if the gain of feedback amplifier is 60dB, the effective gain is just 40dB. To compensate this effect, higher gain is required from the amplifier, while it raise difficulties in low voltage circuit design. The attenuation problem comes from the fact that when the resistive divider tries to scale the output high voltage to the reference level, the AC components are scaled as well. If some method can be used to move the AC components without scaling from the high voltage to a lower one, the problem is solved.
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References


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