0.9V, 5nW, 9ppm/C Resistorless Sub-Bandgap Voltage Reference in 0.18um CMOS

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Outline

• Introduction
• Circuit Description
• Design Methodology
• Simulation Results
• Conclusion
• Acknowledgements
Introduction

Basic Principle of the Bandgap Reference, introduced by Widlar in 1971:

CTAT voltage counterbalance

PTAT voltage

PTAT & CTAT: proportional and complementary to absolute temperature
Circuit Description
Circuit Description – BJT Bias

- Sweep VG1;
- Mirror Id to the junction;
- Find the crossing point between VG1 and Ve.
Circuit Description – BJT Bias

[Diagram of BJT bias circuit]

DC Op. Point

[Graph showing DC operation point]
Circuit Description – BJT Bias

\[ V_E = \frac{\phi_t}{1 - \frac{1}{m} - \frac{1}{2n}} \left[ 1 + \ln \left( \frac{2eKW}{5L} \frac{I_{SQ}}{I_{SE}} \right) \right] \]

- \( I_{SQ} \) – MOS Specific Current
- \( I_{SE} \) – Junction Reverse Saturation Current
- \( V_{TO} \) – Threshold Voltage
- \( n \) – MOS subthreshold slope
- \( m \) – BJT non-ideality factor
- \( W \) – MOS width
- \( L \) – MOS length
- \( \phi_T \) – Thermal Voltage
Circuit Description – BJT Bias

\[ V_E = \frac{\phi_t}{1 - \frac{1}{m}} [1 + \ln \left( \frac{2eKW ISQ}{5L I_{SE}} \right) - \frac{V_{T0}}{n\phi t}] \]

< 0dB
Stable

LASCAS’2014 - 0.9V, 5nW, 9ppm/°C Resistorless Sub-Bandgap Voltage Reference in 0.18um CMOS
Circuit Description – Self-Cascode

- Both transistors are in weak inversion;
- $M_{\text{HIGH}}$ is in saturation;
- $M_{\text{LOW}}$ can be in saturation or in triode.

$$V_{DS(\text{LOW})} = n\phi_t \ln \left( \frac{I_{\text{LOW}}S_{\text{HIGH}}}{I_{\text{HIGH}}S_{\text{LOW}}} \right)$$

Circuit Description – Sub-BGR

Bias Circuit
Circuit Description – Sub-BGR

3 Self-Cascode Cells
Circuit Description – Sub-BGR

\[ V_{REF} = V_{GS1} + V_{PTAT} = \frac{V_E}{2} + n\phi_t \ln \left( 60 \frac{S_3S_5S_7}{S_2S_4S_6} \right) \]

-1mV/°C

+1mV/°C
Design Methodology

• Junction voltage of 550 mV – 3.5 nA;
  • At least 500 pA @ 27°C for ID of every MOSFET;
  • Balance the SC PTAT cells contribution;
  • Round numbers for current mirror and SC PTAT aspect ratio gains;
  • Standard transistors with VB = 0.
Simulation Results - Layout

Area = 0.0012 mm² in 0.18um XFAB
Simulation Results - Temperature

(a) $V_{REF}$

(b) Voltages (V)

(c) Currents (nA)

TC = 8.79 ppm/°C for 0 – 125°C

5 nW @ 27°C, 18 nW @ 125°C
Simulation Results – Power Supply

LS = 2.112 mV/V and 69pA/V
For VDD = 0.85 - 1.8 V

PSRR @ 100 Hz = -48dB
VDD = 0.9 V
Simulation Results – Variability

**Average Process Variation**

- **VREF**
  - $\mu = 479.5 \text{ mV}$
  - $\sigma = 9.57 \text{ mV}$

- **TC**
  - $\mu = 479.5 \text{ mV}$
  - $\sigma = 3.851 \text{ mV}$

**Local Random Variation**

- $\sigma / \mu = 2\%$ die-to-die
- $\sigma / \mu = 0.8\%$ within-die

- Yield = 96% for TC < 50 ppm/°C
## Simulation Results – Comparison

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<td>0.5</td>
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<td>52.5</td>
<td>4.86</td>
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All papers are experimental results, except for this work. The best case result was chosen for comparison in all works.

[8] – Ming et. al. TCAS II, 2010
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<td>Power Supply</td>
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<td>0.5-3.6</td>
<td>0.7-1.8</td>
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<td>V</td>
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<td>PSRR @ 100Hz</td>
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<td>Area</td>
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<td>0.043</td>
<td>0.0014</td>
<td>0.0246</td>
<td>0.0012</td>
<td>mm²</td>
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Conclusion

- Presented a nano-Watt sub-bandgap voltage ref;
- New BJT bias topology and self-cascode PTAT cells;
- Achieves 9 ppm/°C for the 0 – 125°C temp. range;
  - 5 nW @ 27°C and 0.9 V;
- Very small area of 0.0012 mm².
Conclusion

• Average process variation is main cause for variability;
  • 2% sigma/mean process variation for $V_{\text{ref}}$;
    • 96% yield for a TC < 50 ppm/°C;
  • Re-designed with similar results on IBM 0.13um.
  • Sent to fabrication on 18 February 2014.
Acknowledgments

• CI-BRASIL Program for licensing XFAB 0.18um PDK and financial support;
• MOSIS Educational Program for licensing IBM 0.13um PDK and fabrication;