ICs for Chip Cards

Intelligent 1K-Byte EEPROM SLE 4418/SLE 4428

Short Product Information

February 1995

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	Editorial Changes

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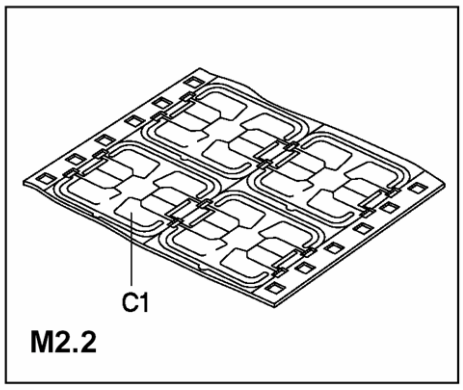
Intelligent1K-Byte EEPROM with Write Protect Function **SLE4418**

Intelligent 256-Byte EEPROM with Write Protect Function and Programmable Security Code (PSC) **SLE4428**



Features

- 1024 x 8 bit EEPROM organization
- Byte-wise addressing
- Irreversible byte-wise write protection
- 1024 x 1 bit protection memory organization
- Serial three-wire bus
- End of programming indicated on data output
- Minimum of 10^4 write/erase cycles
- Data retention for minimum of ten years
- Contact configuration and serial interface in accordance to ISO standard 7816 (synchronous transmission)

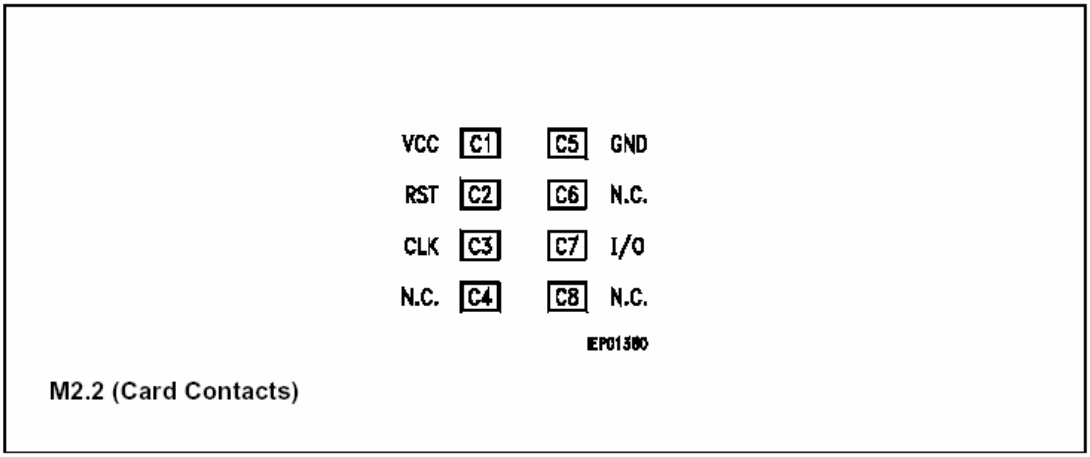
Additional Feature of SLE 4428

- Data can only be changed after entry of the correct 2-byte programmable security code (PSC)

Type	Ordering Code	Package
SLE 4418 C	on request	Chip
SLE 4418 M2.2	on request	Wire-Bonded Module M2.2
SLE 4428 C	on request	Chip
SLE 4428 M2.2	on request	Wire-Bonded Module M2.2

1 Pin Configuration

(top view)



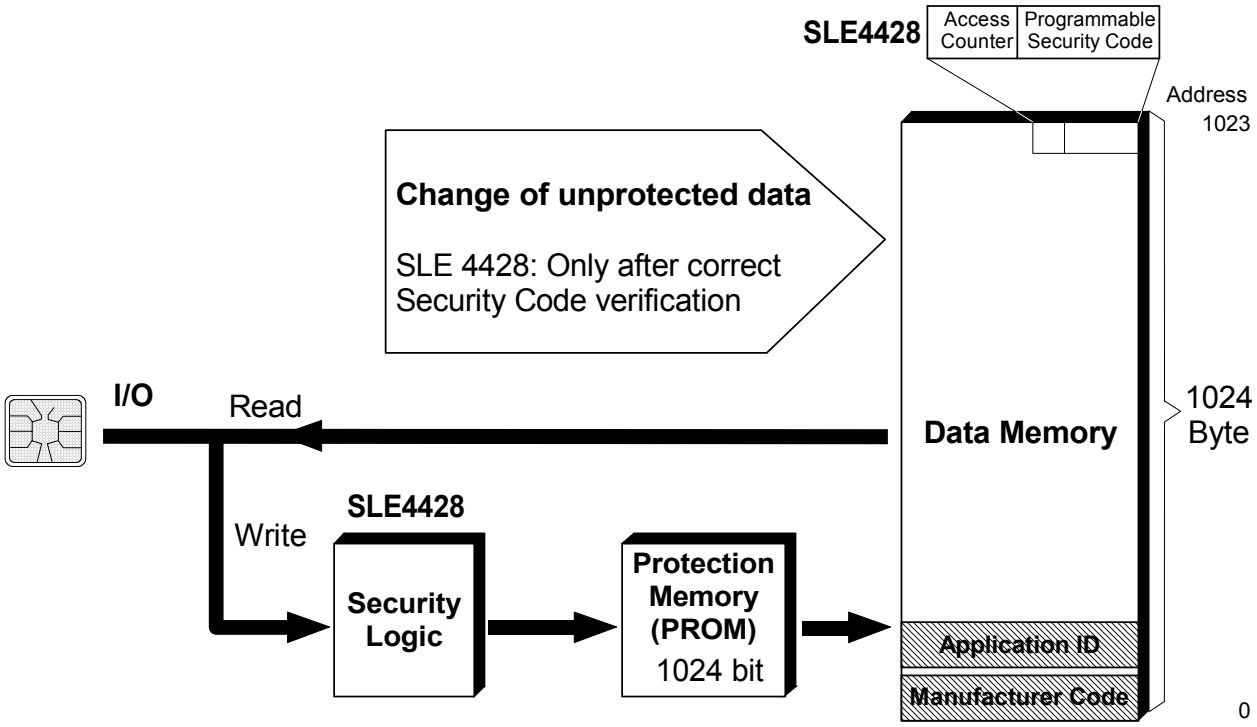
M2.2 (Card Contacts)

Pin Definitions and Functions

Card Contact	Symbol	Function
C1	VCC	Supply voltage
C2	RST	Reset
C3	CLK	Clock input
C4	N.C.	Not connected
C5	GND	Ground
C6	N.C.	Not connected
C7	I/O	Bidirectional data line (open drain)
C8	N.C.	Not connected

SLE 4418/SLE 4428 comes as a M2.2 wire-bonded module for embedding in plastic cards or as a die for customer packaging.

Memory Map SLE 4418/28



SLE 4418

The SLE 4418 consists of 1024 x 8 bit EEPROM main memory and a 32-bit protection memory with PROM functionality. The main memory is erased and written byte by byte. When erased, all 8 bits of a data byte are set to logical one. When written, the information in the individual EEPROM cells is, according to the input data, altered bit by bit to logical zeros (logical AND between the old and the new data in the EEPROM). Normally a data change consists of an erase and write procedure. It depends on the contents of the data byte in the main memory and the new data byte whether the EEPROM is really erased and/or written. If none of the 8 bits in the addressed byte requires a zero-to-one transition the erase access will be suppressed. Vice versa the write access will be suppressed if no one-to-zero transition is necessary. The write and the erase operation takes at least 2.5 ms each.

Each of the first 32 bytes can be irreversibly protected against data change by writing the corresponding bit in the protection memory. Each data byte in this address range is assigned to one bit of the protection memory and has the same address as the data byte in the main memory which it is assigned to. Once written the protection bit cannot be erased (PROM).

SLE 4428

Additionally to the above functions the SLE 4418 provides a security code logic which controls the write/erase access to the memory. For this purpose the SLE 4428 contains a 4-byte security memory with an Error Counter EC (bit 0 to bit 2) and 3 bytes reference data. These 3 bytes as a whole are called Programmable Security Code (PSC). After power on the whole memory, except for the reference data, can only be read. Only after a successful comparison of verification data with the internal reference data the memory has the identical access functionality of the SLE4418 until the power is switched off. After three successive unsuccessful comparisons the Error Counter blocks any subsequent attempt, and hence any possibility to write and erase.

2.2Transmission Protocol
The transmission protocol is a two wire link protocol between the interface device IFD and the integrated circuit IC. It is identical to the protocol type “S=A”. All data changes on I/O are initiated by the falling edge on CLK.

The transmission protocol consists of the 4 modes:
–Reset and Answer-to-Reset
–Command Mode
–Outgoing Data Mode
–Processing Mode

Note:The I/O pin is open drain and therefore requires an external pull up resistor to achieve a high level.

Command Mode

The SLE 4418 provides 4 commands which are listed in table 1. Additionally to these commands the SLE 4428 provides 3 commands which can be found in table 2

Table 1

Byte 1 Control								Byte 2 Address	Byte 3 Data	Operation	Mode
B7	B6	B5	B4	B3	B2	B1	B0	A7-A0	D7-D0		
0	0	1	1	0	0	0	0	address	no effect	READ MAIN MEMORY	outgoing data
0	0	1	1	1	0	0	0	address	input data	UPDATE MAIN MEMORY	processing
0	0	1	1	0	1	0	0	no effect	no effect	READ PROTECTION MEMORY	outgoing data
0	0	1	1	1	1	0	0	address	input data	WRITE PROTECTION MEMORY	processing

Table 2
SLE 4442 only

0	0	1	1	0	0	0	1	no effect	no effect	READ SECURITY MEMORY	outgoing data
0	0	1	1	1	0	0	1	address	input data	UPDATE SECURITY MEMORY	processing
0	0	1	1	0	0	1	1	address	input data	COMPARE VERIFICATION DATA	processing

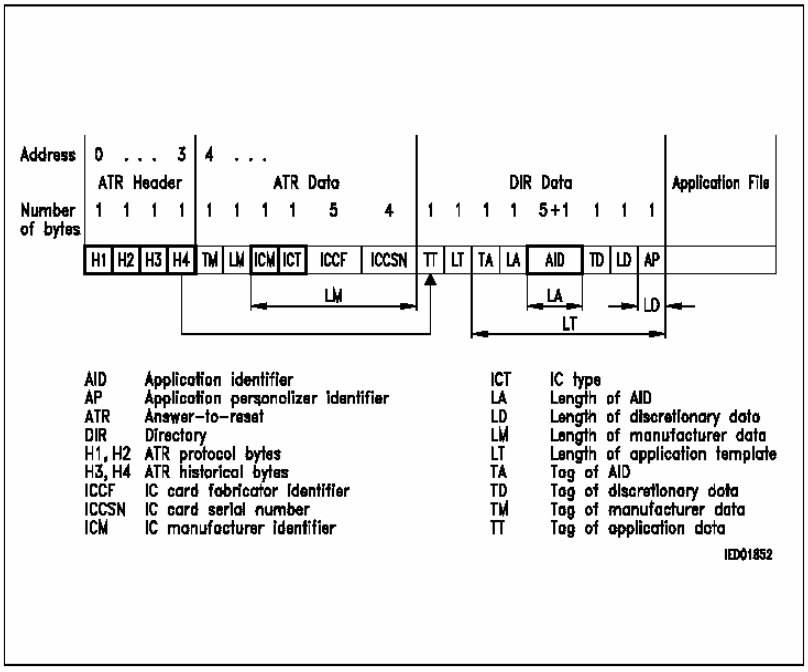


Figure 12
ATR and Directory Data of Structure

3 Operational Information

3.1 Memory Map

Address (decimal)	Main Memory	Protection Memory	Security Memory
255	Data Byte 255 (D7 … D0)		
:	:		
32	Data Byte 32 (D7 … D0)		
31	Data Byte 31 (D7 … D0)	Protection Bit 31 (D31)	
:	:	:	
3	Data Byte 3 (D7 … D0)	Protection Bit 3 (D3)	Reference Data Byte 3 (D7 … D0)
2	Data Byte 2 (D7 … D0)	Protection Bit 2 (D2)	Reference Data Byte 2 (D7 … D0)
1	Data Byte 1 (D7 … D0)	Protection Bit 1 (D1)	Reference Data Byte 1 (D7 … D0)
0	Data Byte 0 (D7 … D0)	Protection Bit 0 (D0)	Error Counter (0,0,0,0,0,D2,D1,D0)

The Data bytes 0 to 31 can be protected against further changes by programming the associated protection bit 0 to 31. The SLE 4442 allows data changing only after correct verification of the Reference Data bytes. Reading of the Data bytes and of the associated protection bits is always possible.

3.2 Electrical Characteristics

3.2.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{CC}	– 0.3	6.0	V
Input voltage (any pin)	V_I	– 0.3	6.0	V
Storage temperature	T_{stg}	– 40	125	°C
Power dissipation	P_{tot}		70	mW

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability, including EEPROM data retention and write/erase endurance.

In the operating range the functions given in the circuit description are fulfilled.

3.2.2 Operation Range

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage	V_{CC}	4.75	5.0	5.25	V	–
Supply current	I_{CC}		3	10	mA	V_{CC} = 5 V
Ambient temperature	T_A	0		70	°C	–

3.2.3 DC Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
High level input voltage (I/O, CLK, RST)	V_{IH}	3.5		V_{CC}	V	–
Low level input voltage (I/O, CLK, RST)	V_{IL}	0		0.8	V	–
High level input current (I/O, CLK, RST)	I_{IH}			50	µA	V_{IH} = 5 V
Low level output current (I/O)	I_{OL}	1			mA	V_{OL} = 0.4 V, open drain
High level output current (I/O)	I_{OH}			50	µA	V_{OH} = 5 V, open drain
Input capacitance	C_I			10	pF	